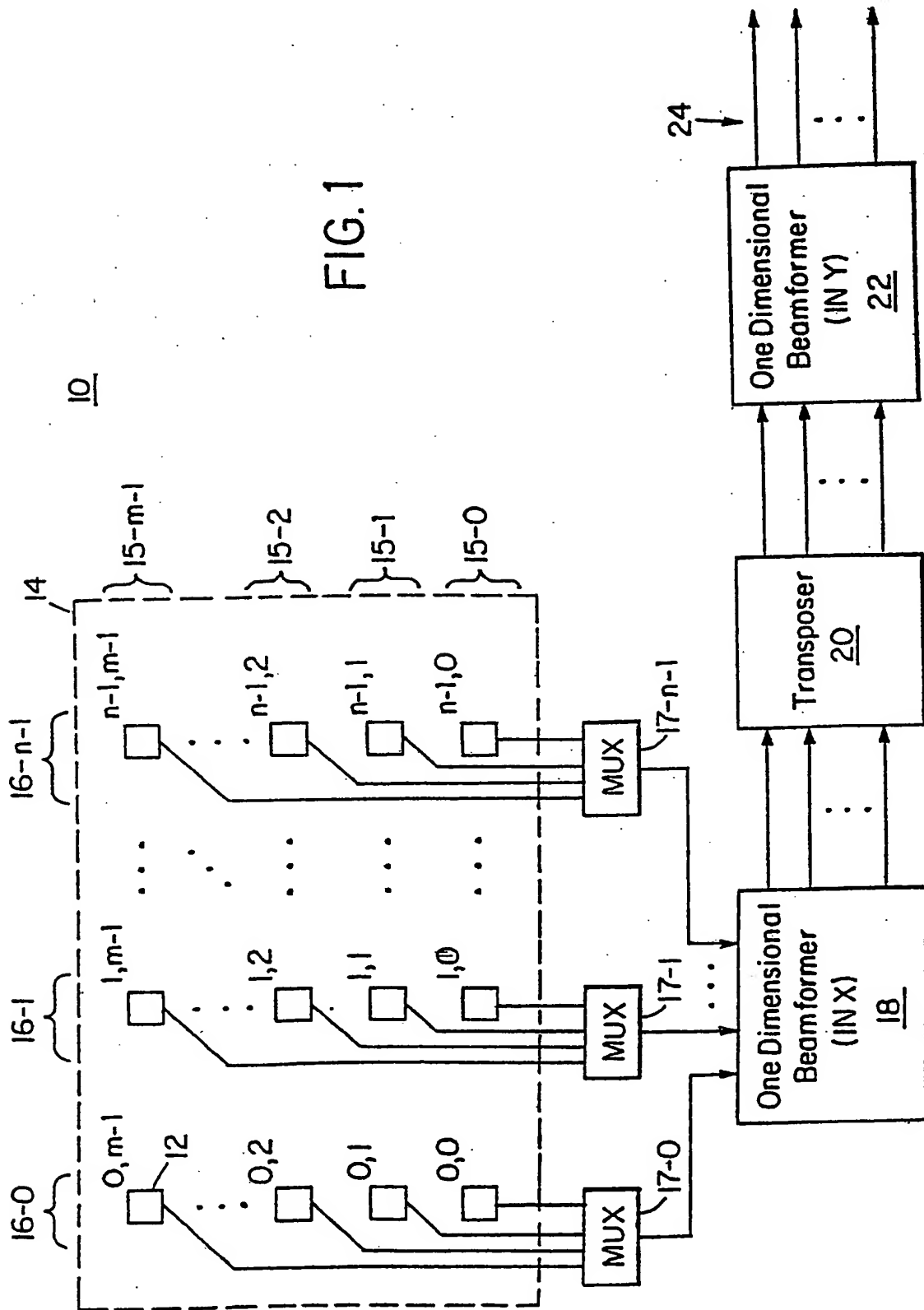


FIG. 1



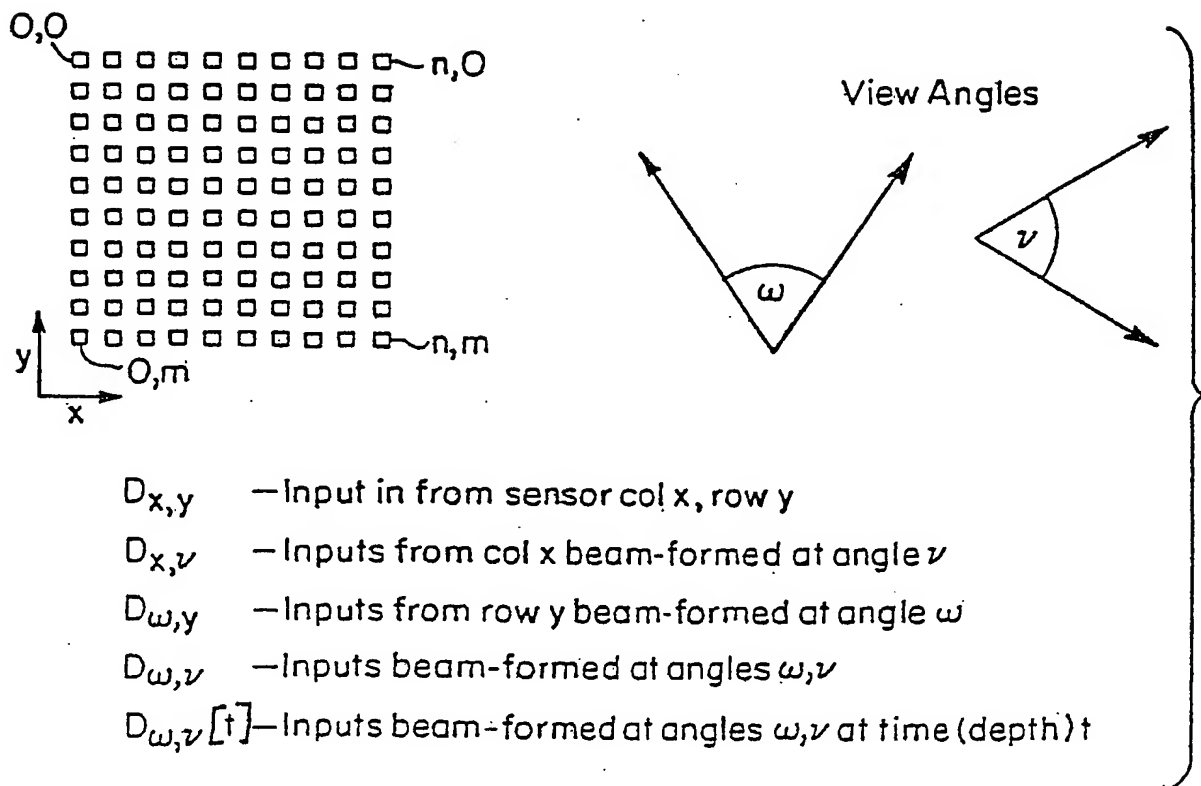


FIG. 2

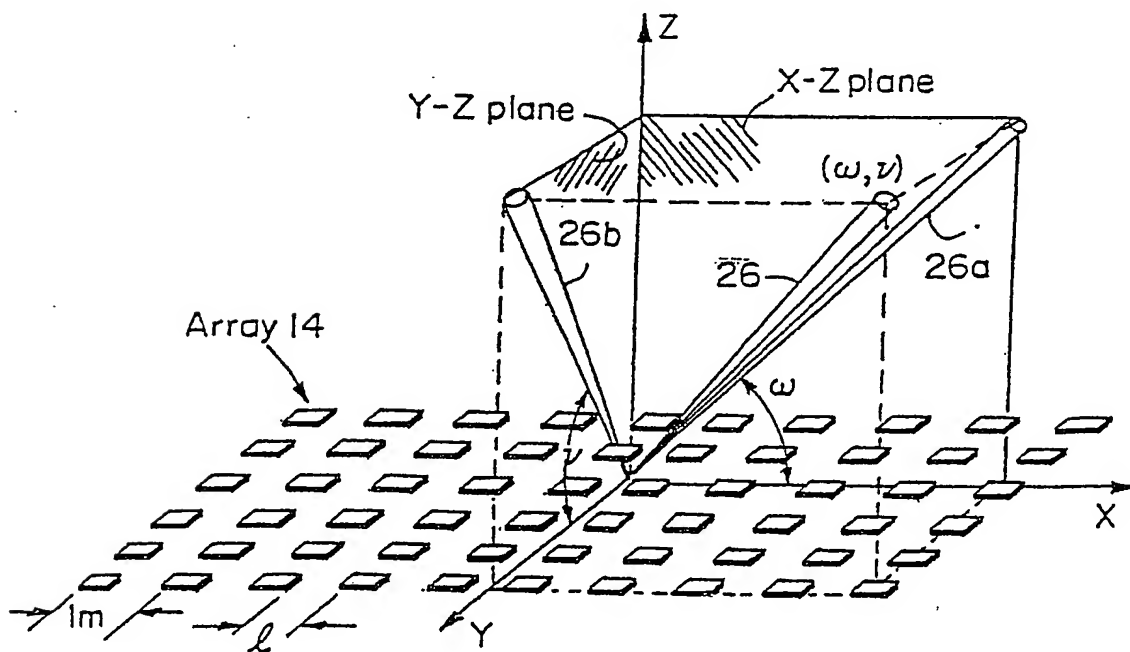


FIG. 3

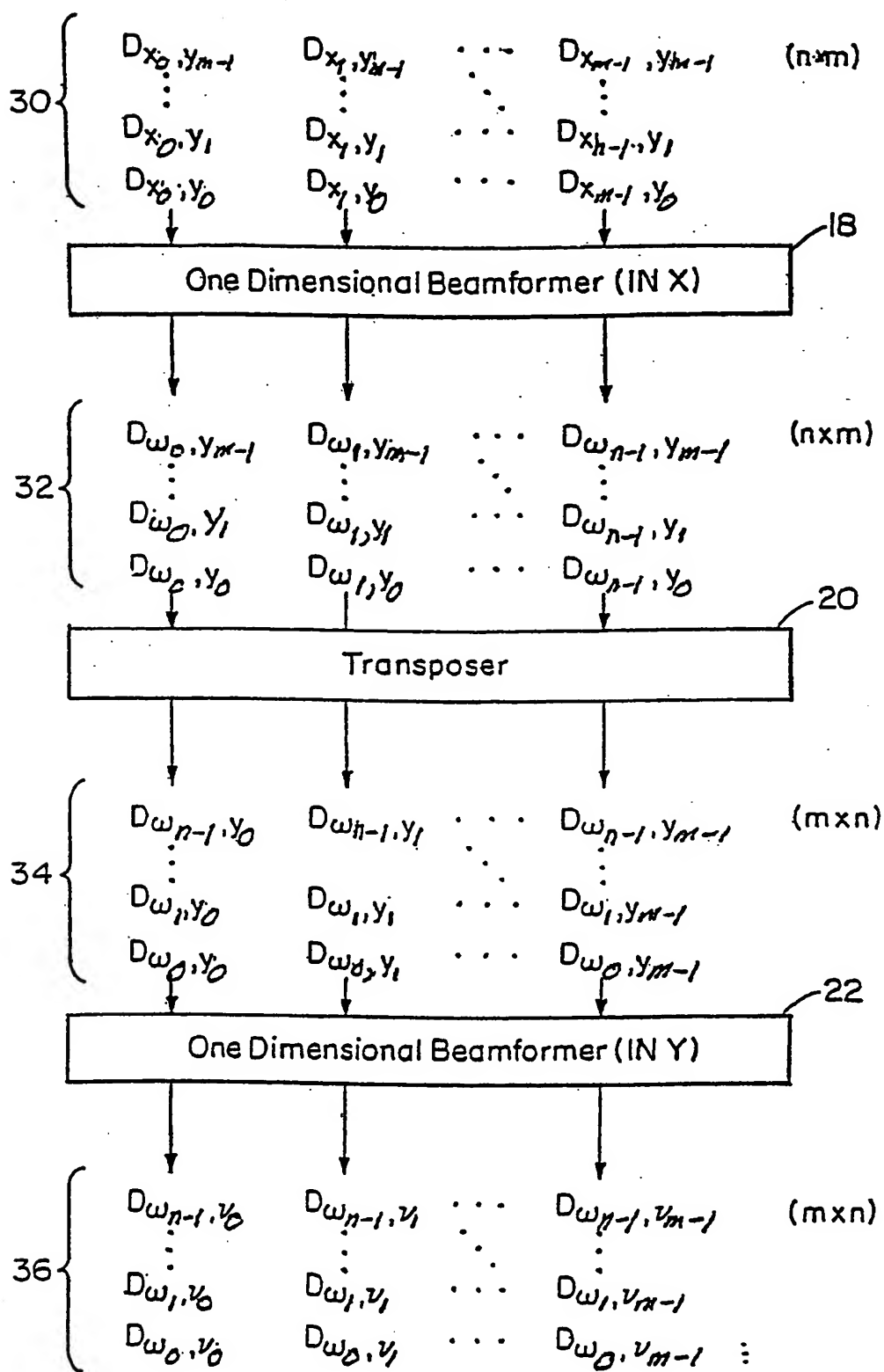


FIG. 4

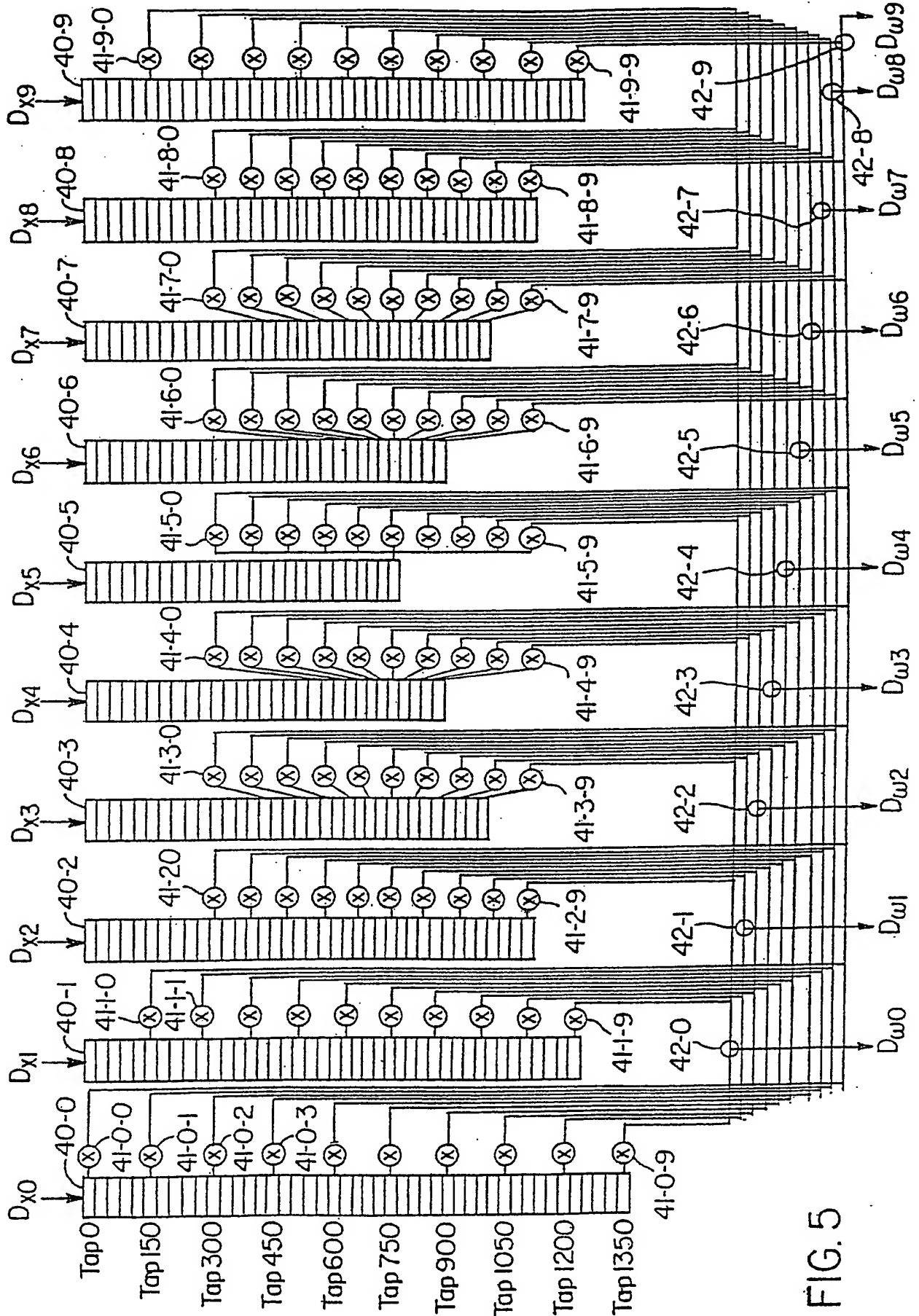


FIG. 5

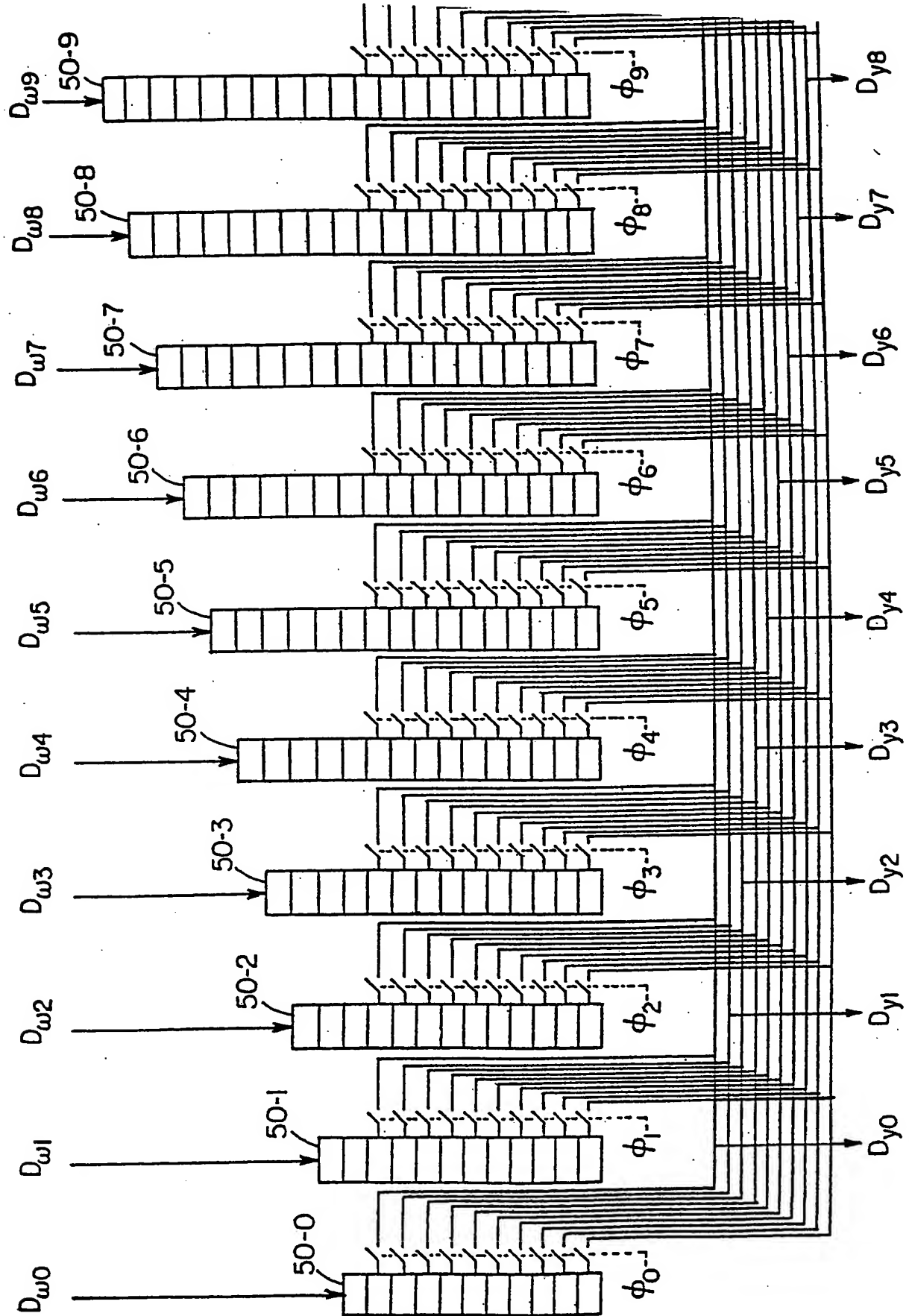
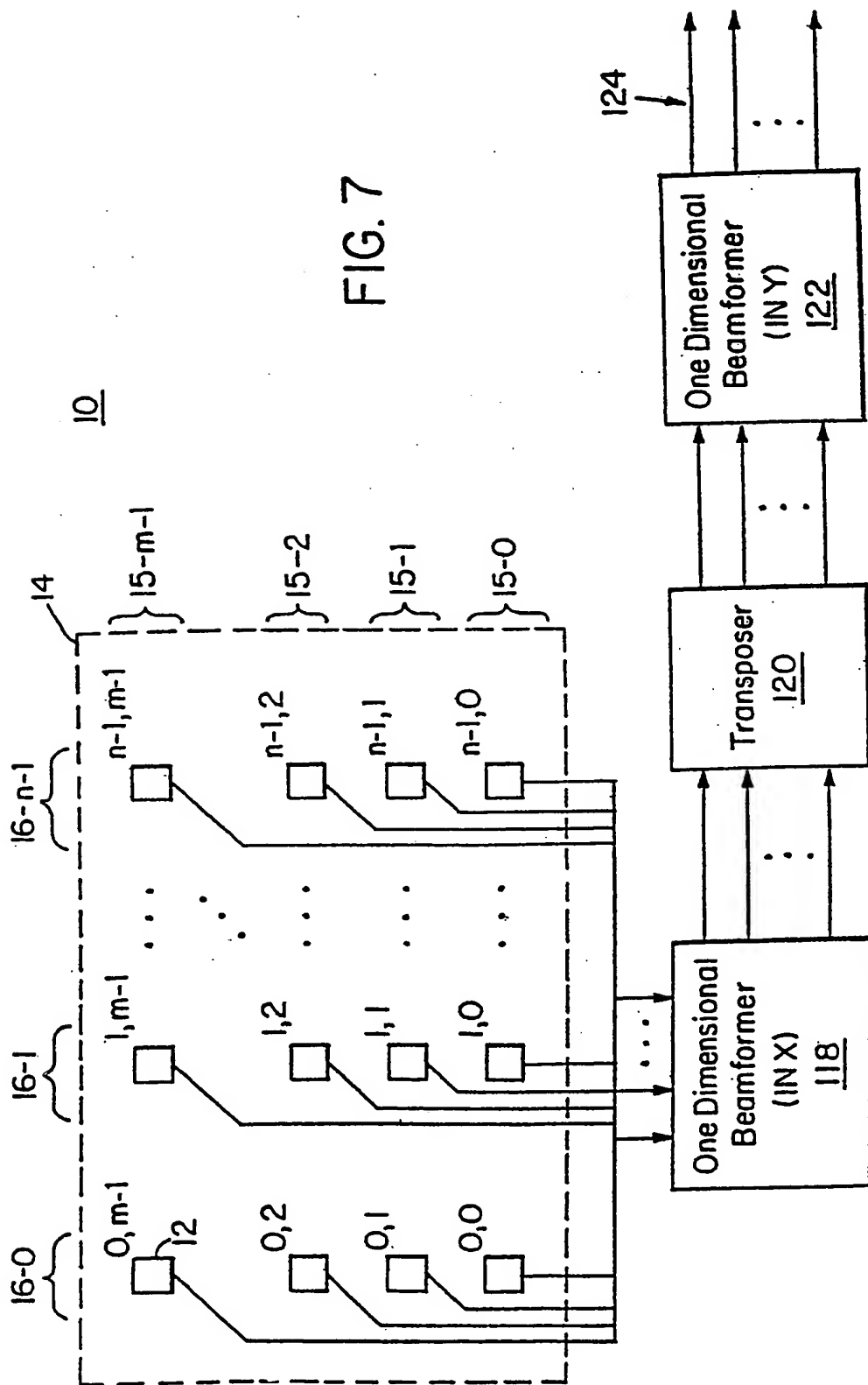


FIG. 6

FIG. 7



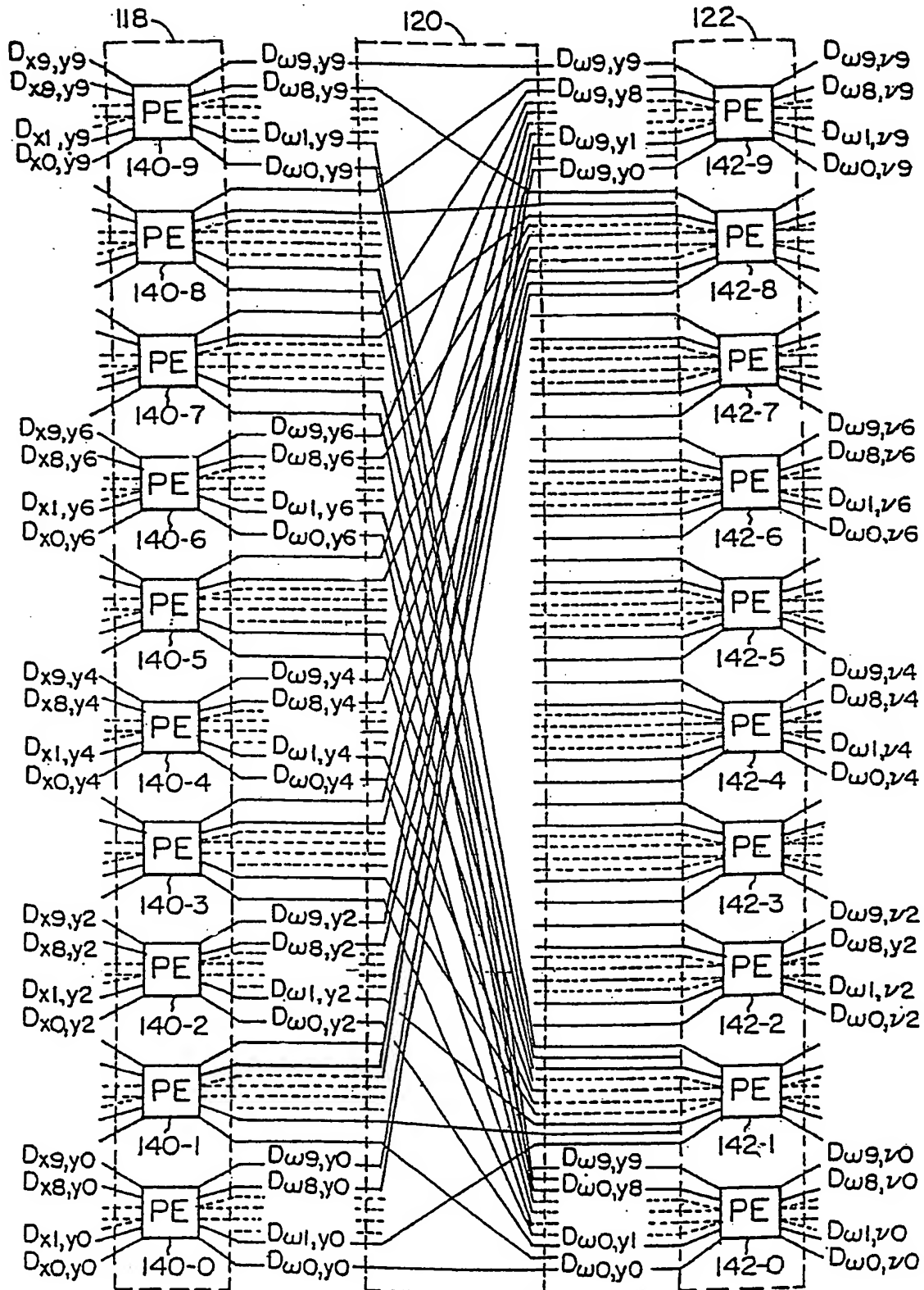


FIG. 8

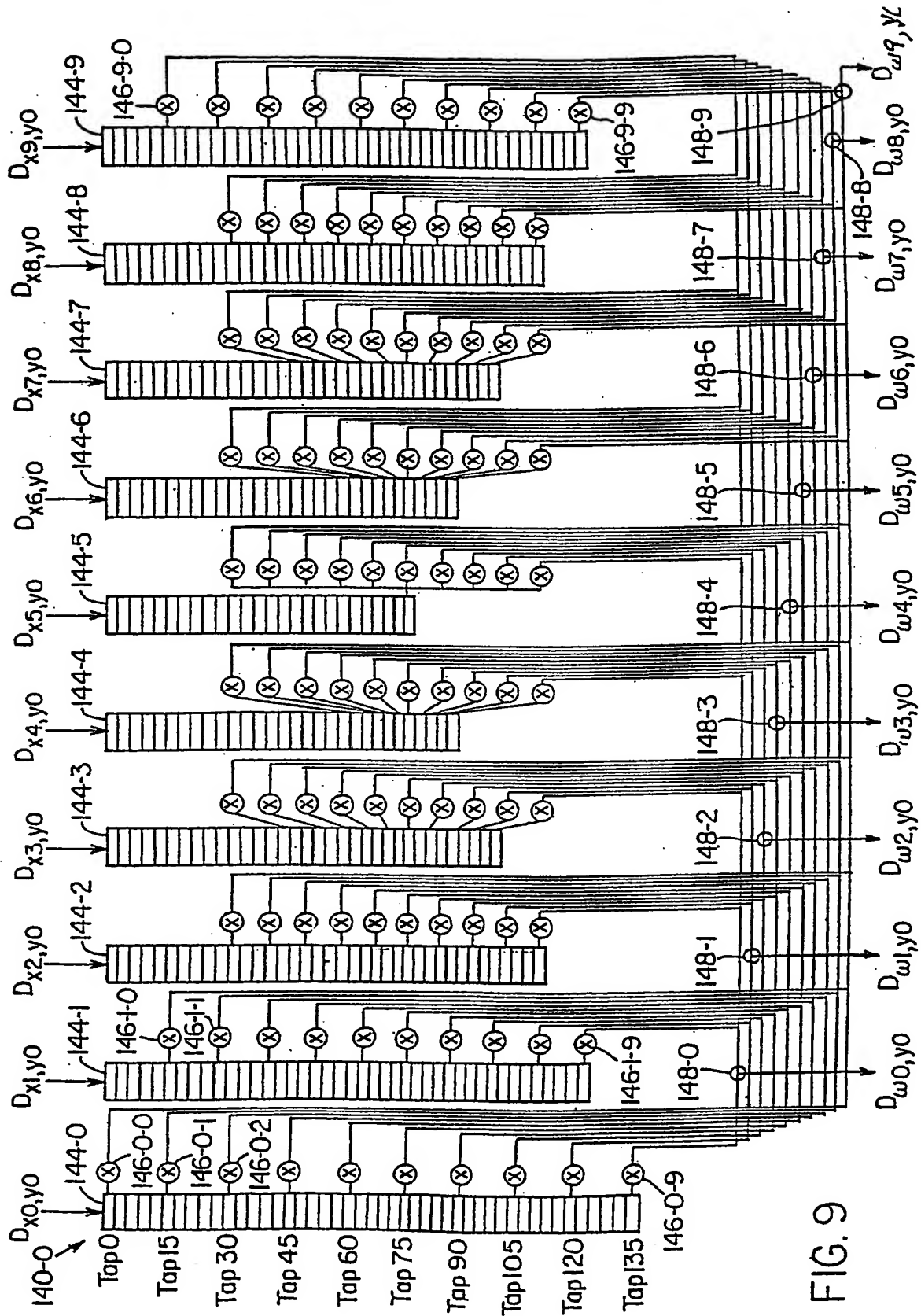
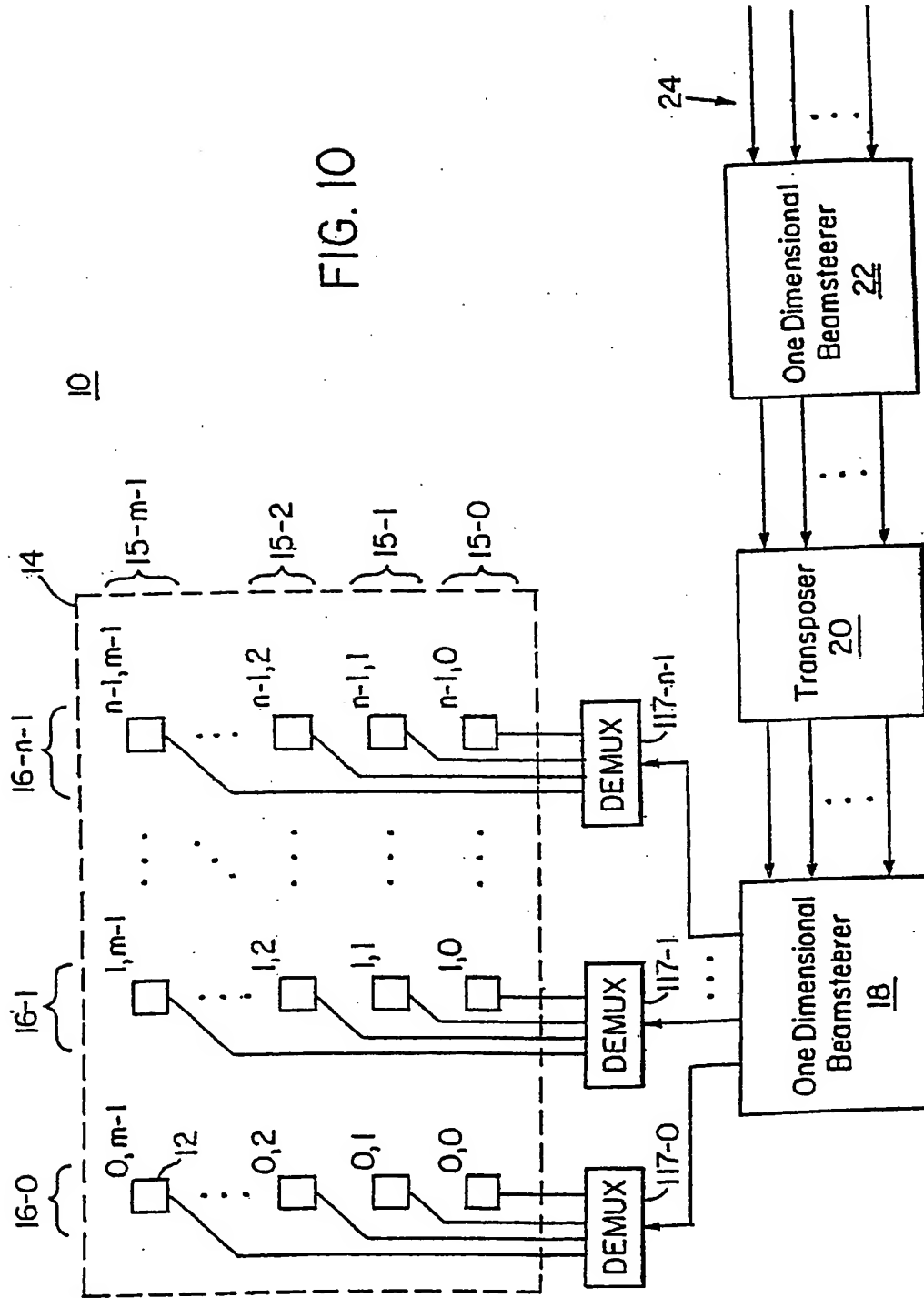
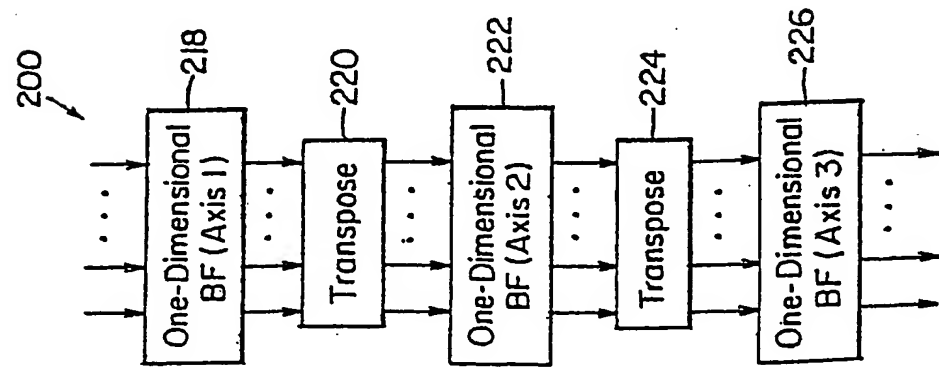
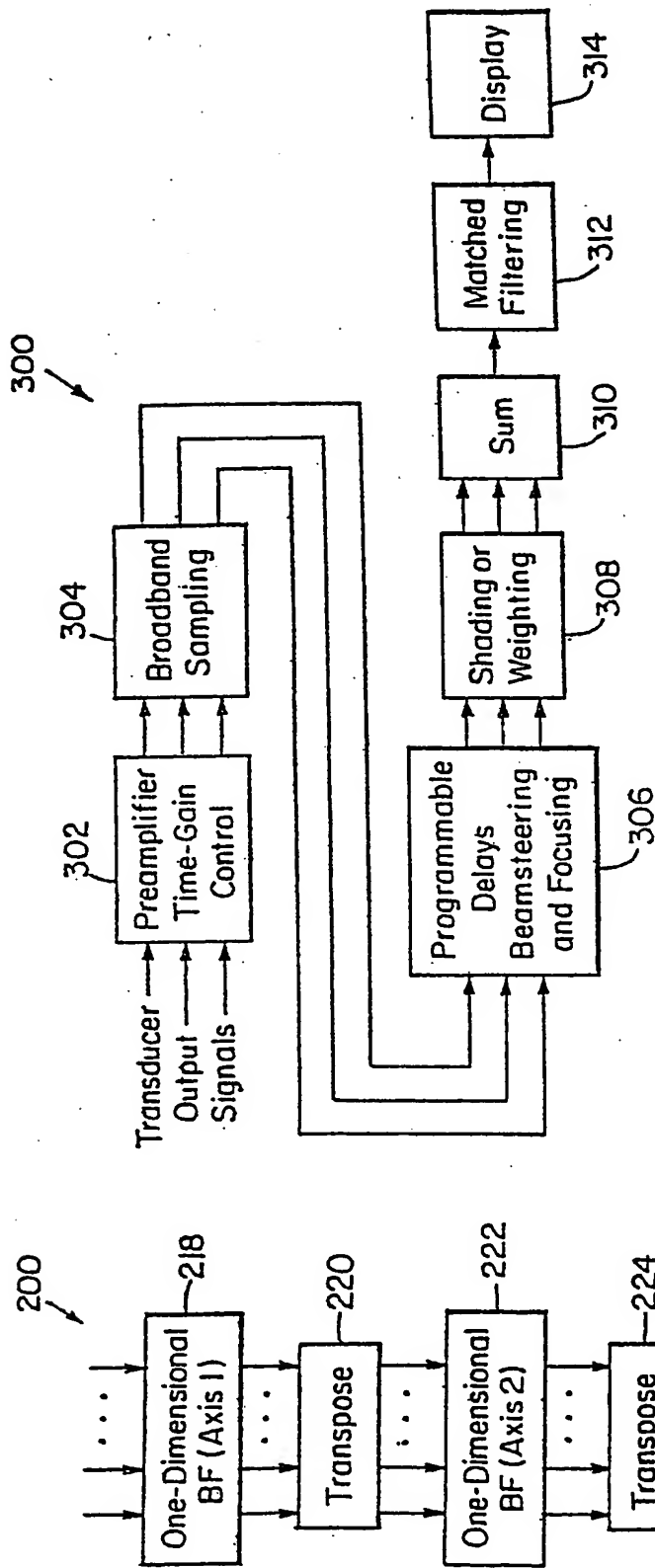


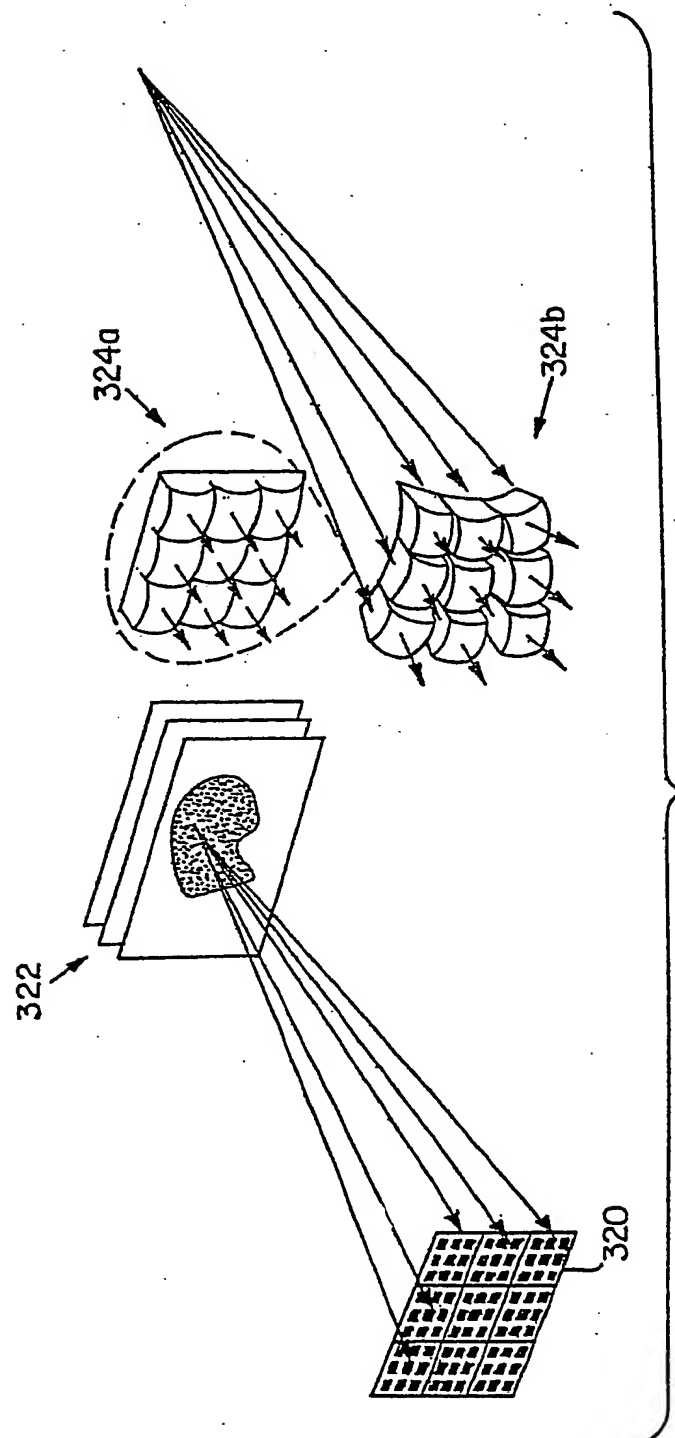
FIG. 9

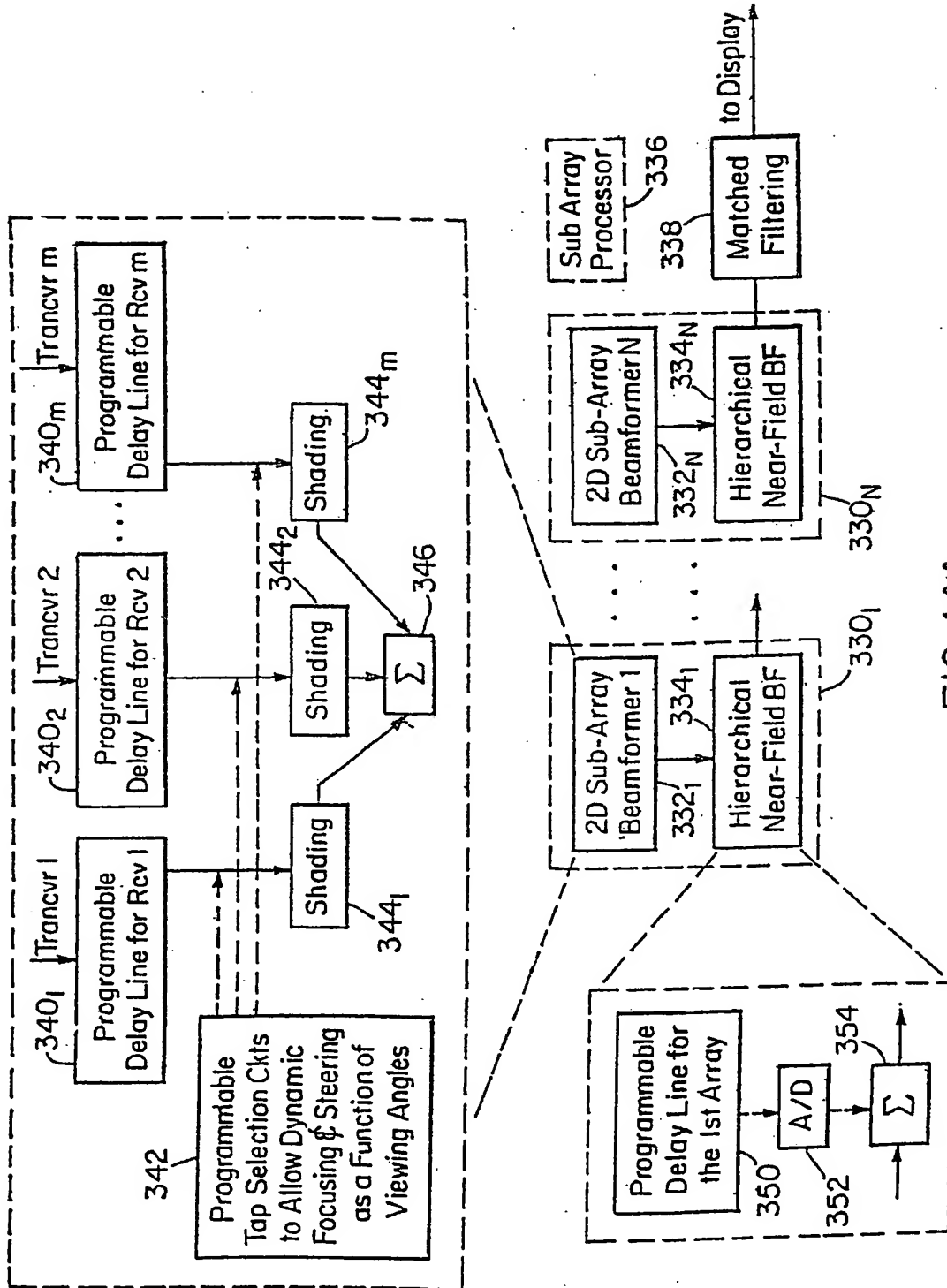


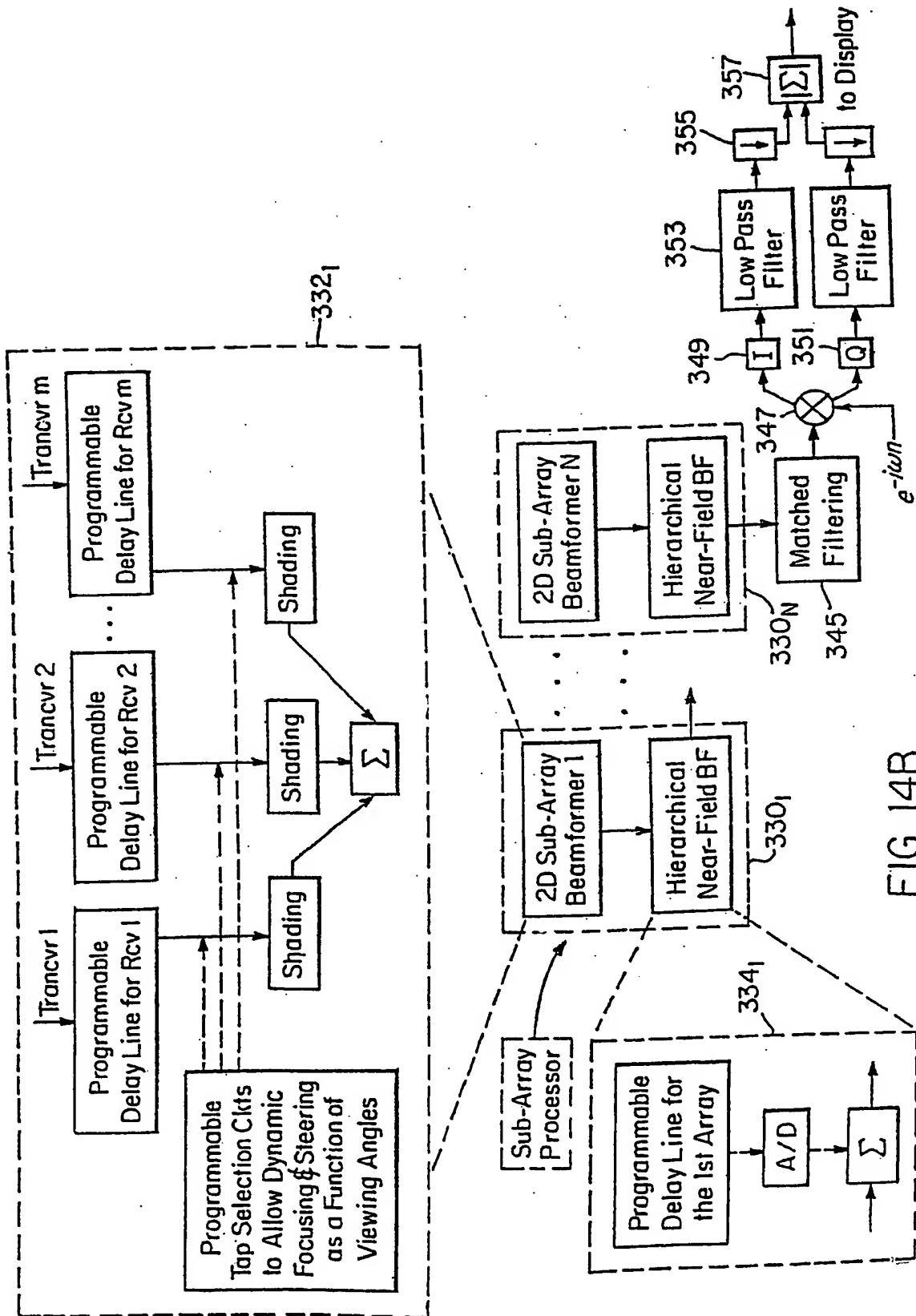
FIG. 10











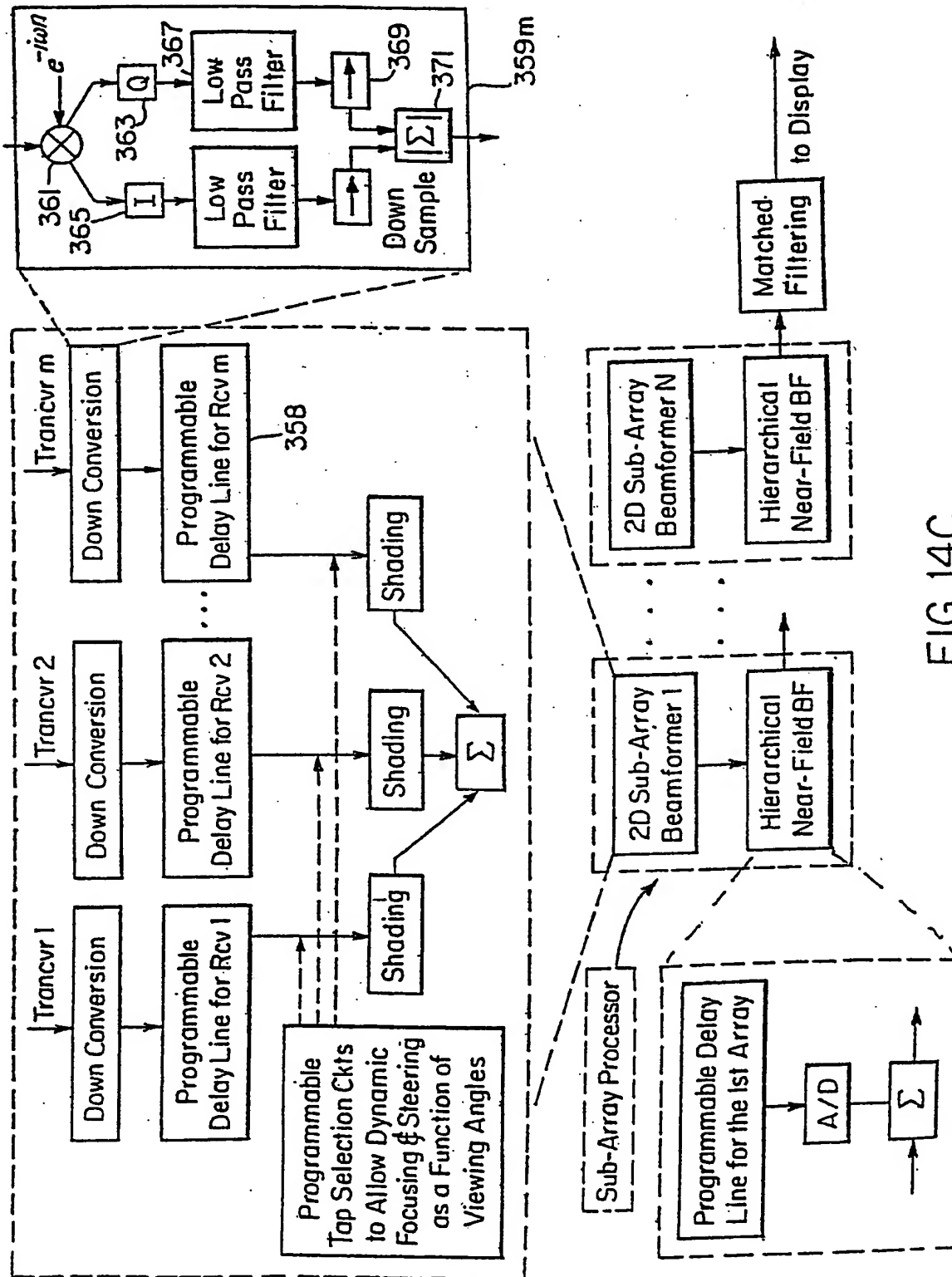
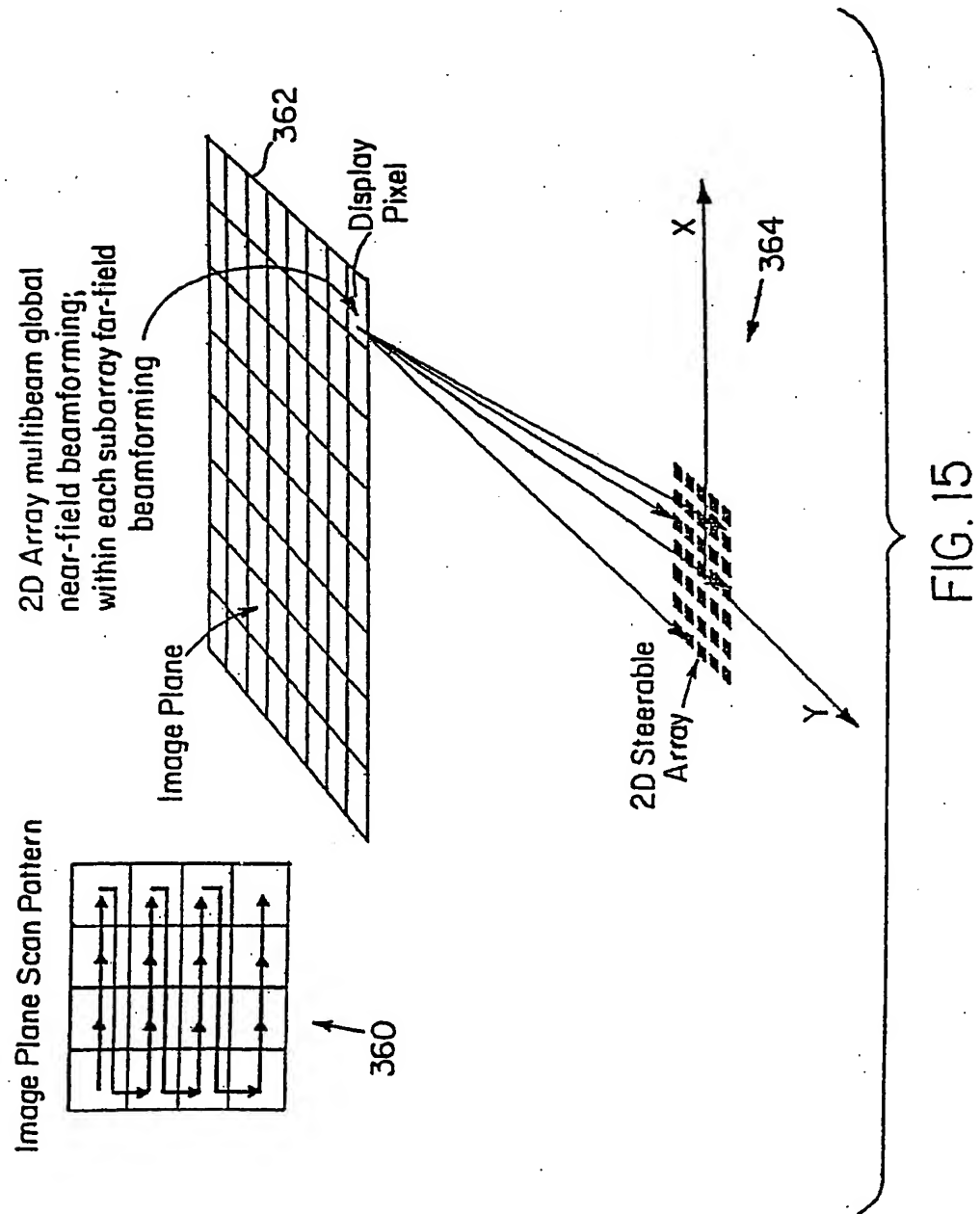
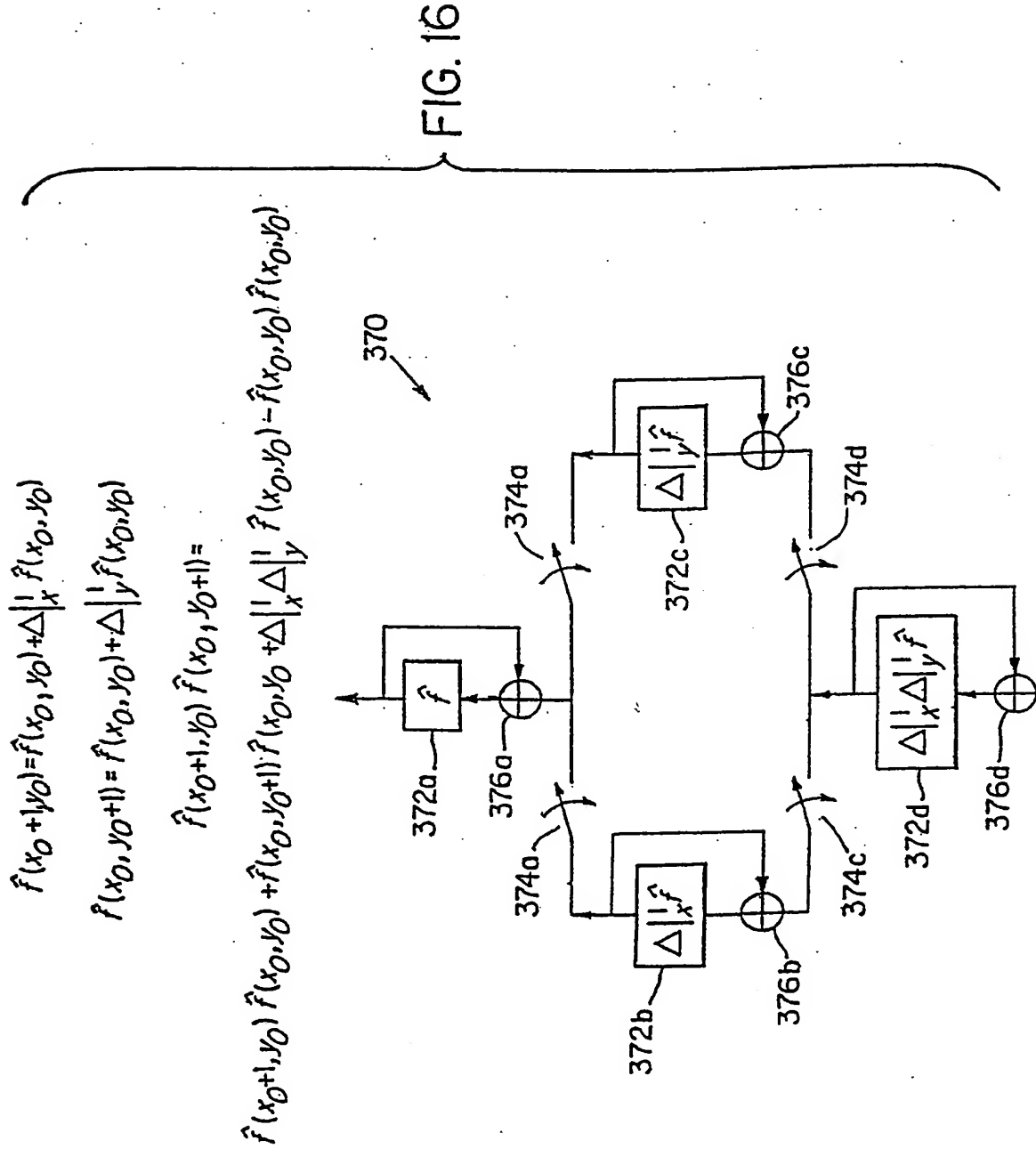


FIG. 14C







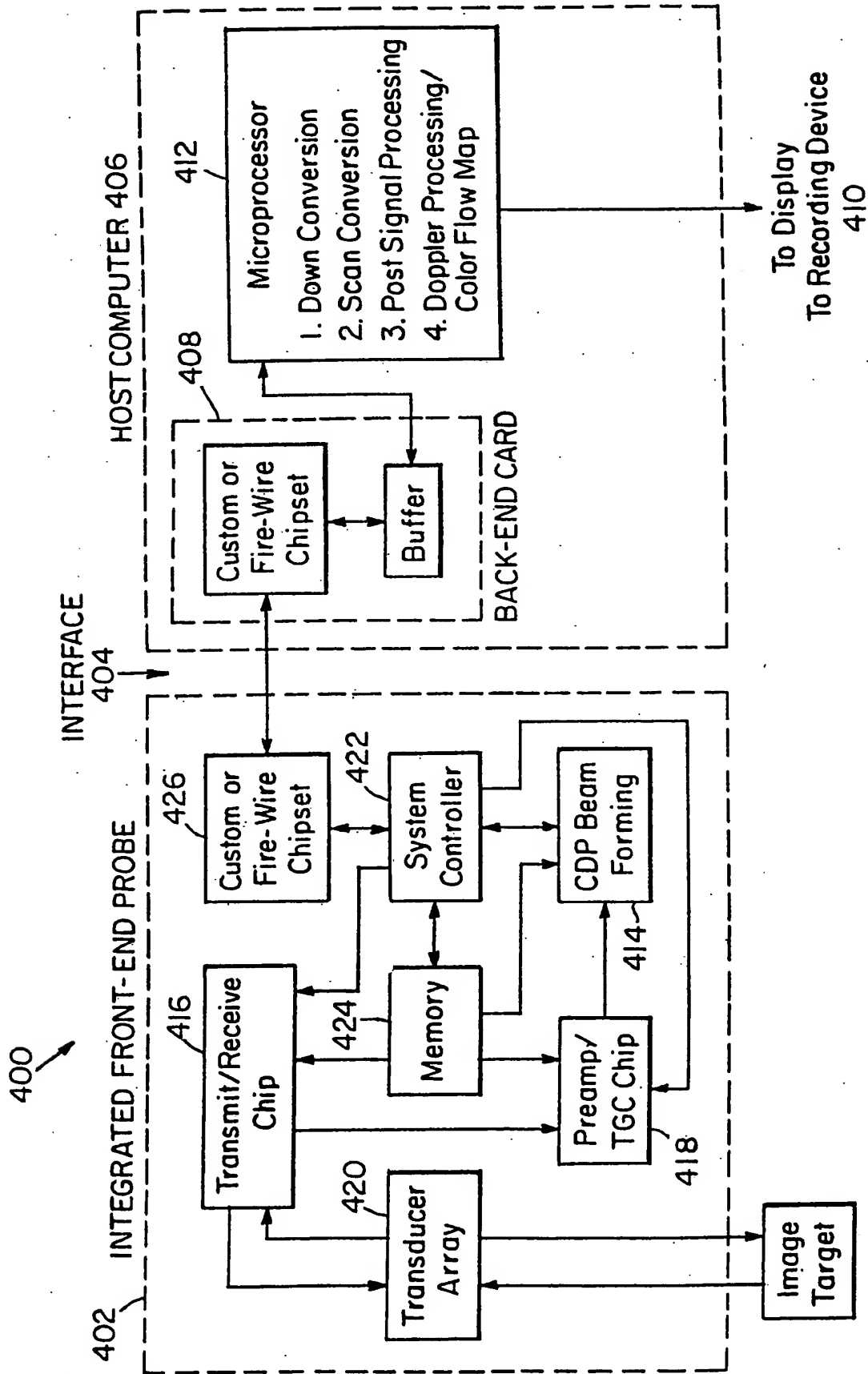


FIG. 17A

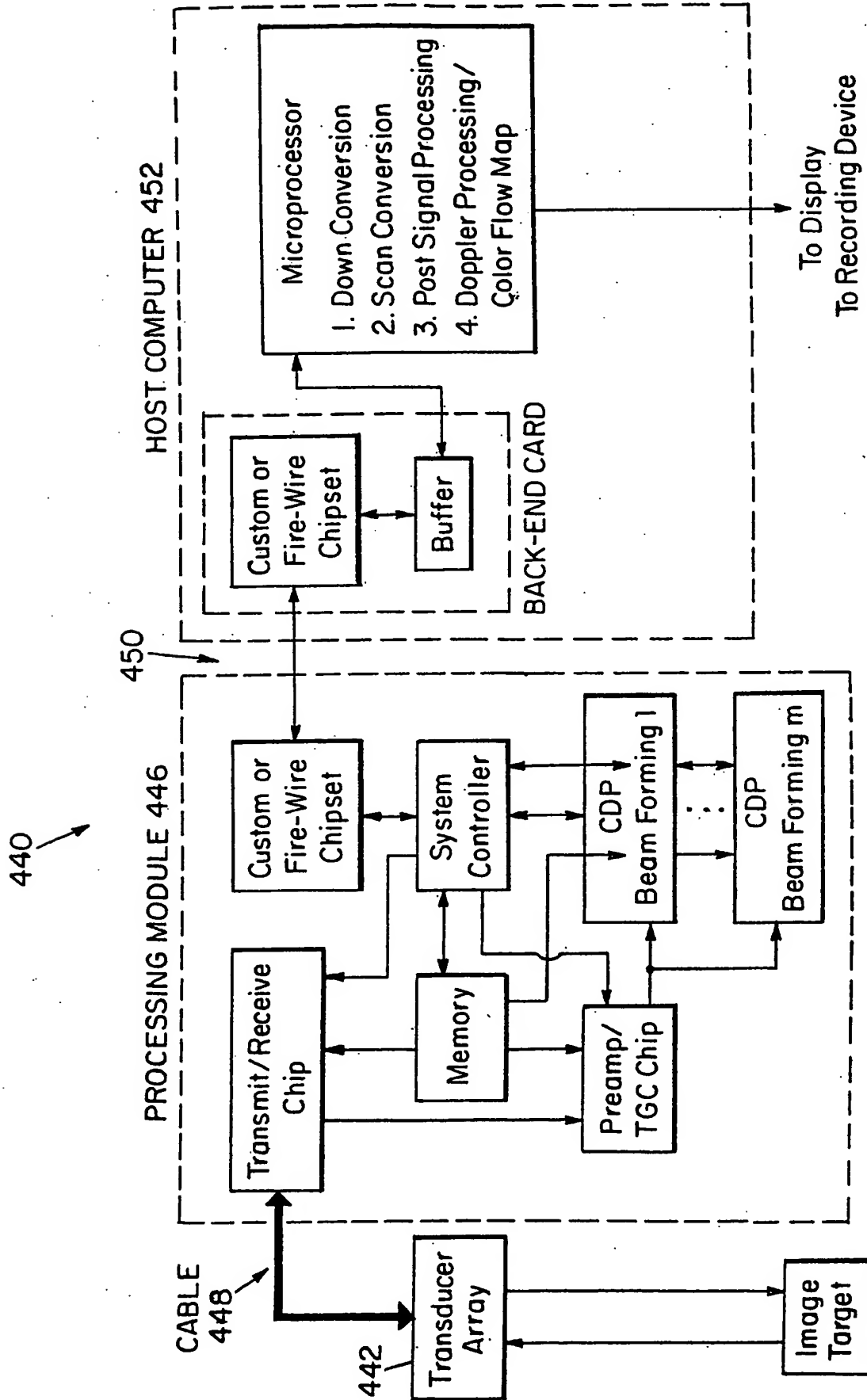


FIG. 17B

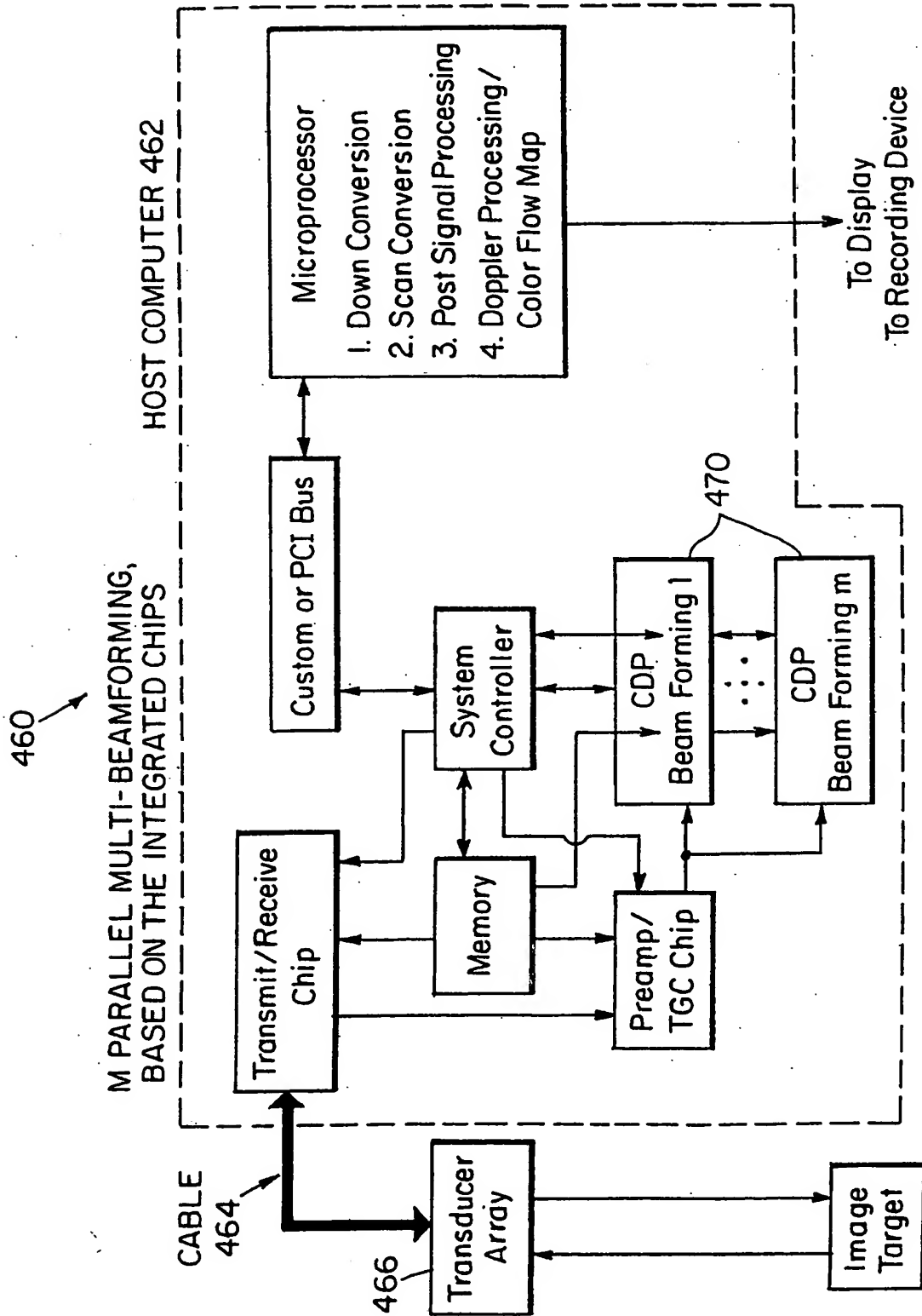


FIG. 17C

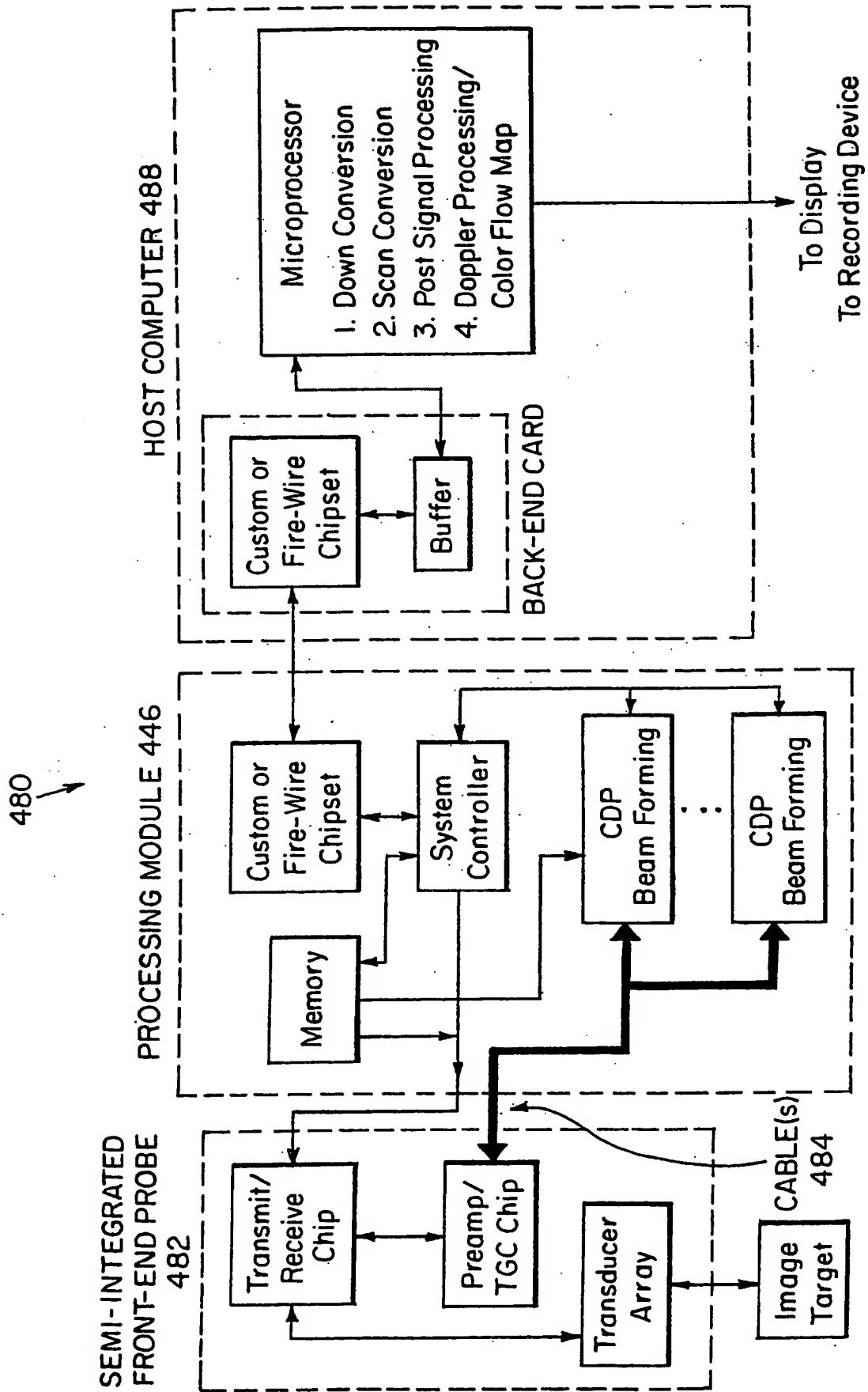


FIG. 17D

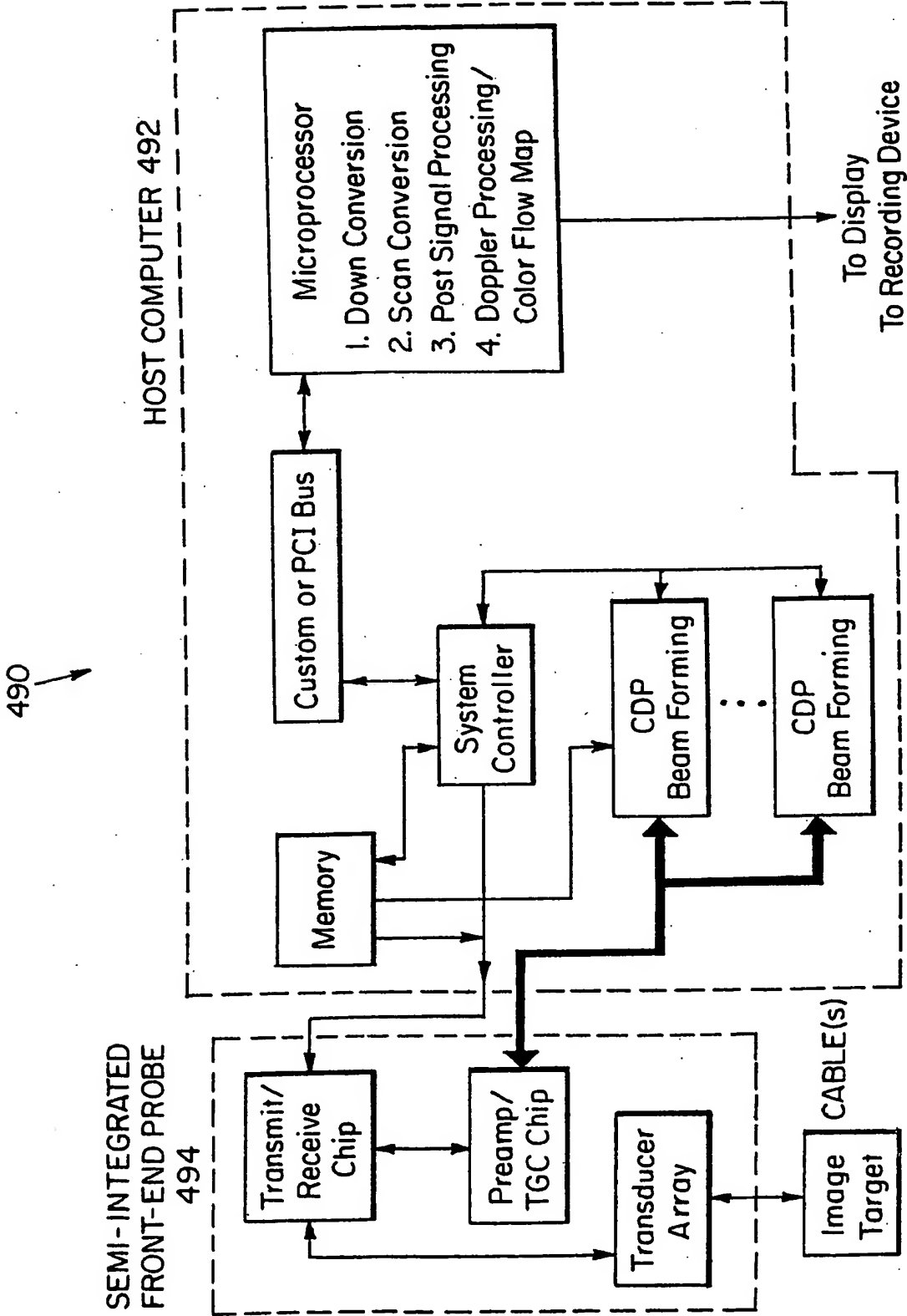
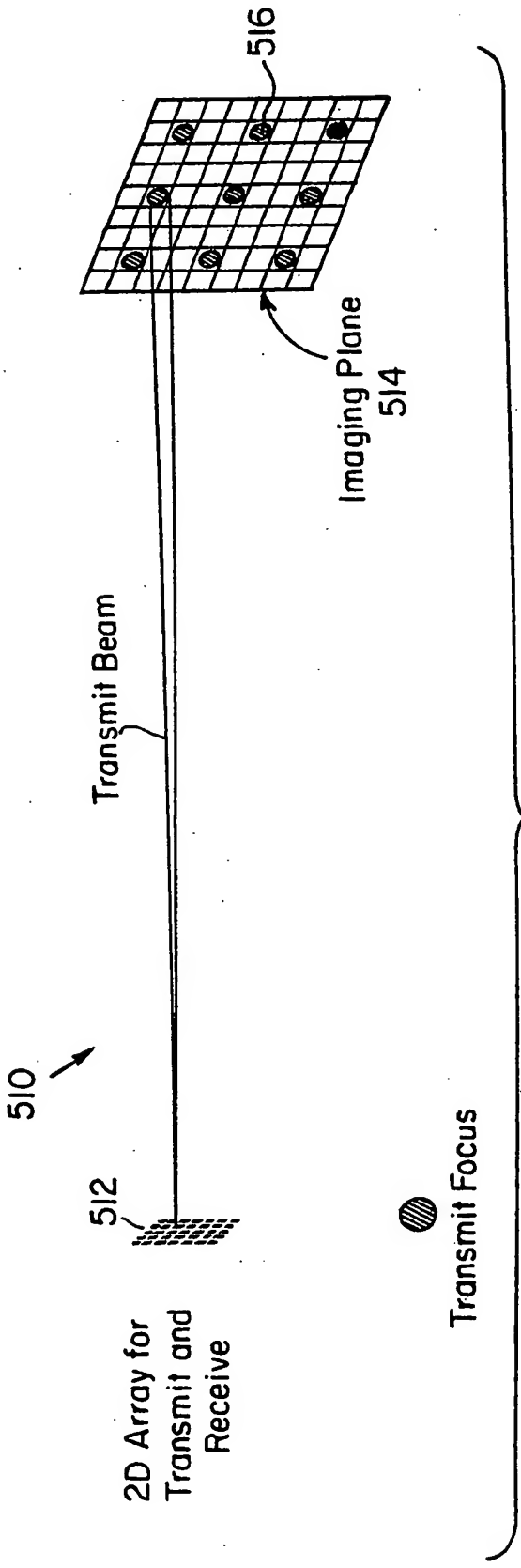
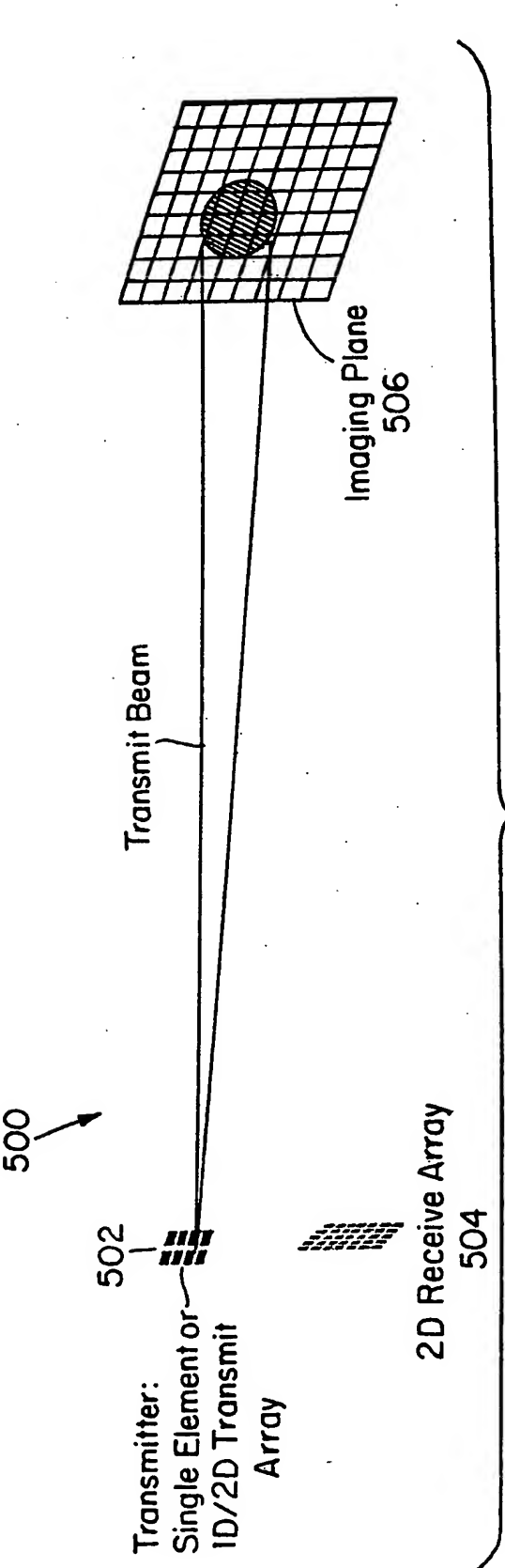


FIG. 17E



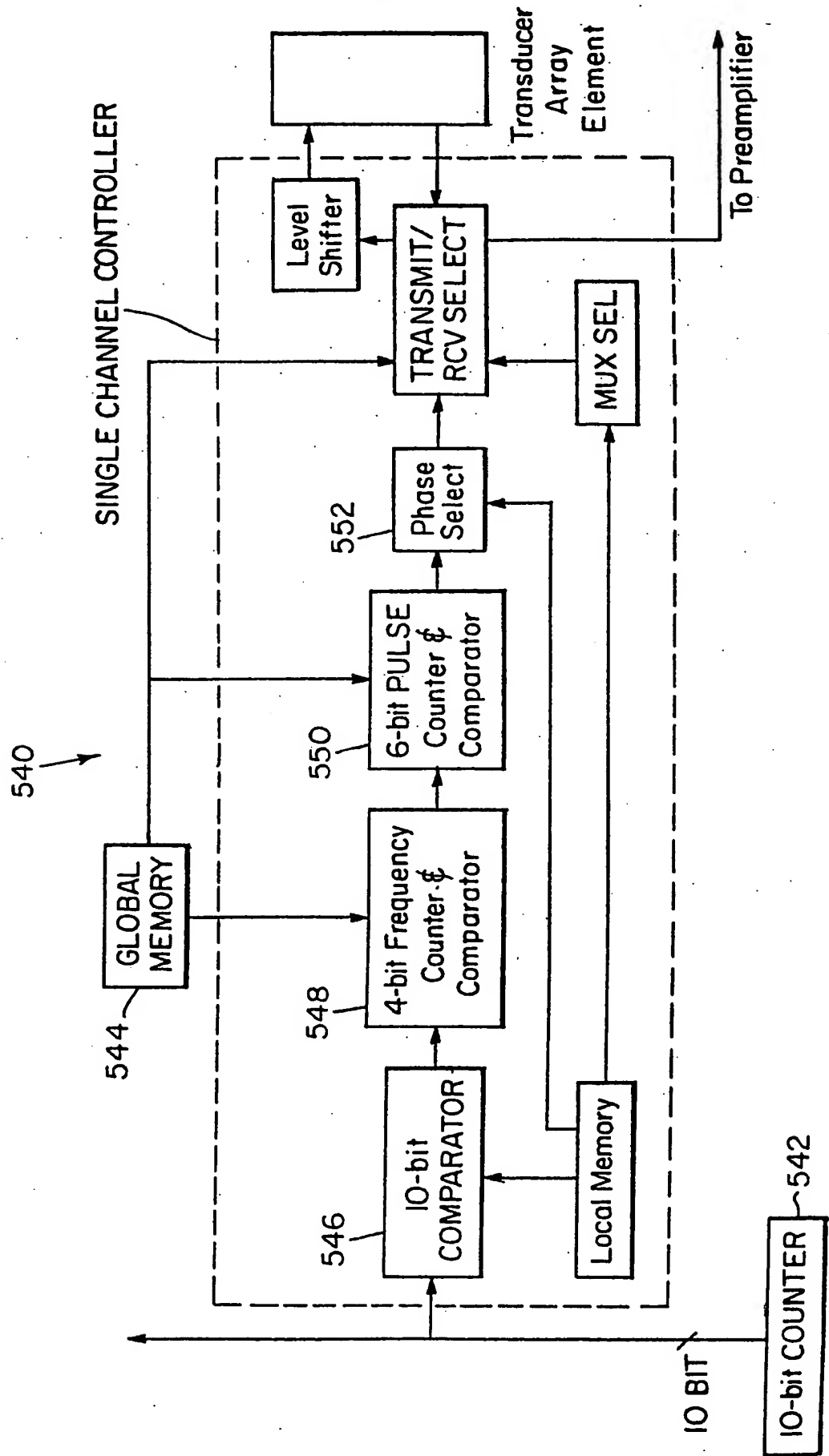


FIG. 19

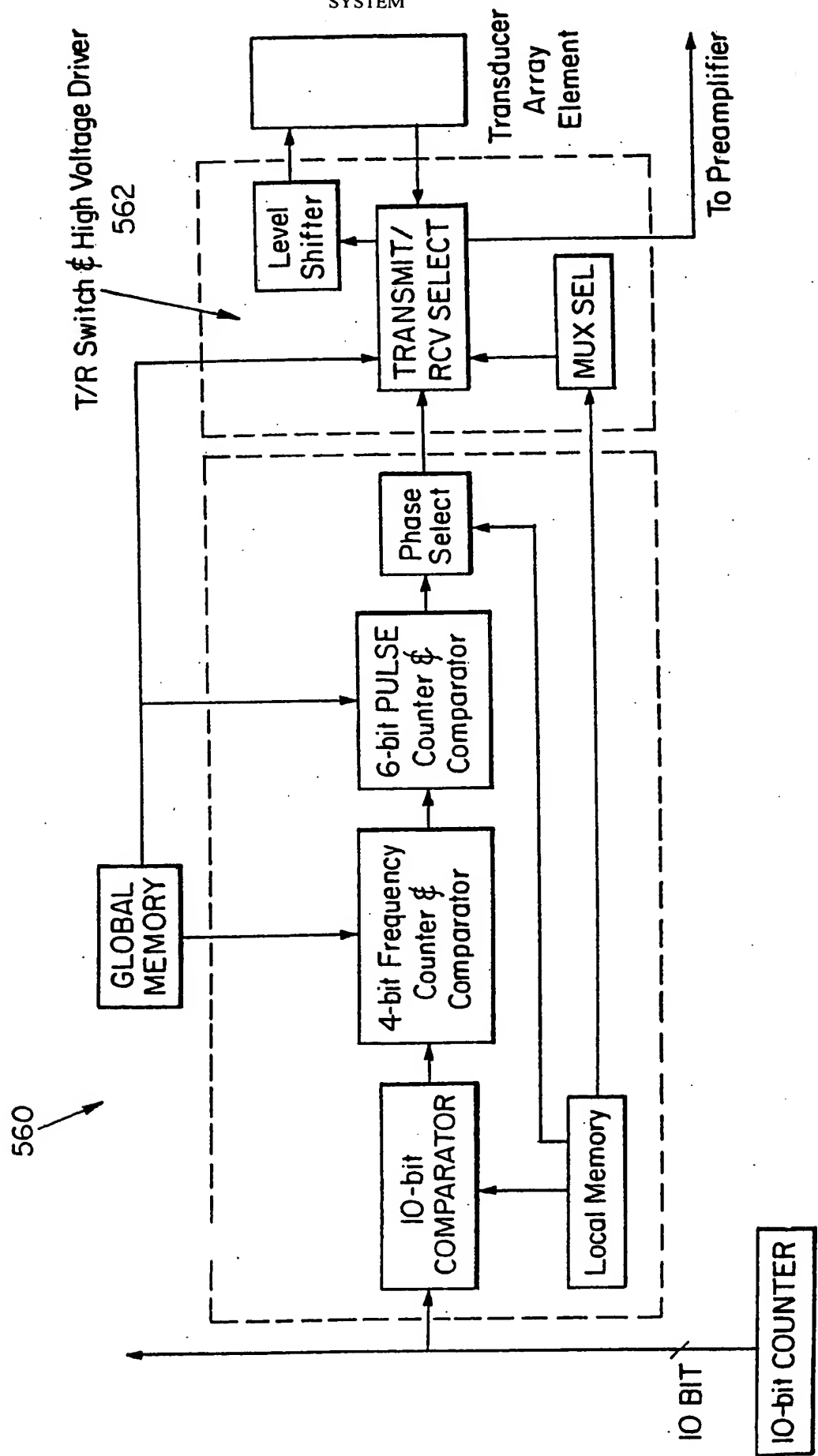


FIG. 20



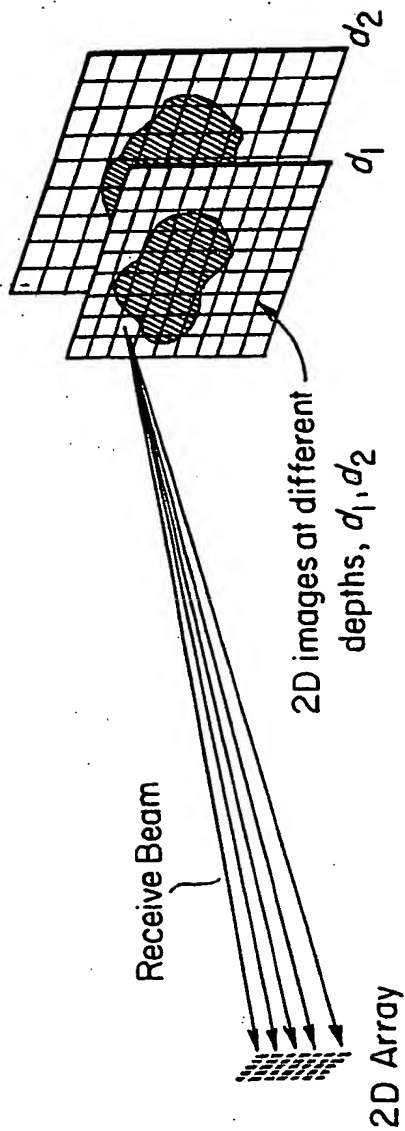


FIG. 21A

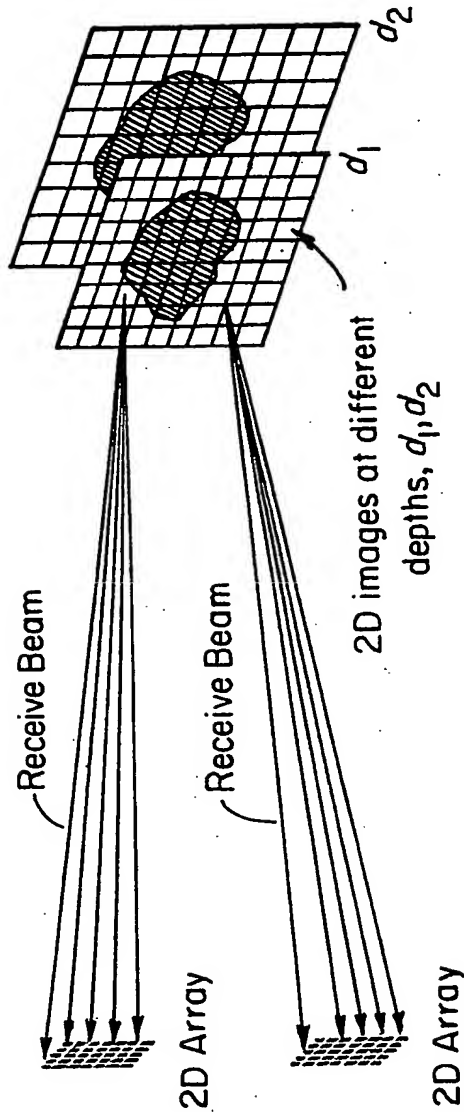


FIG. 21C

Image Plane Scan Pattern

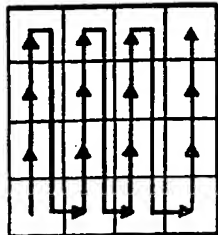


FIG. 21B

Image Plane Scan Pattern

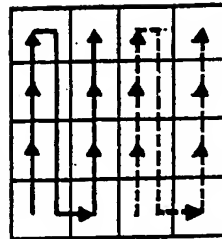
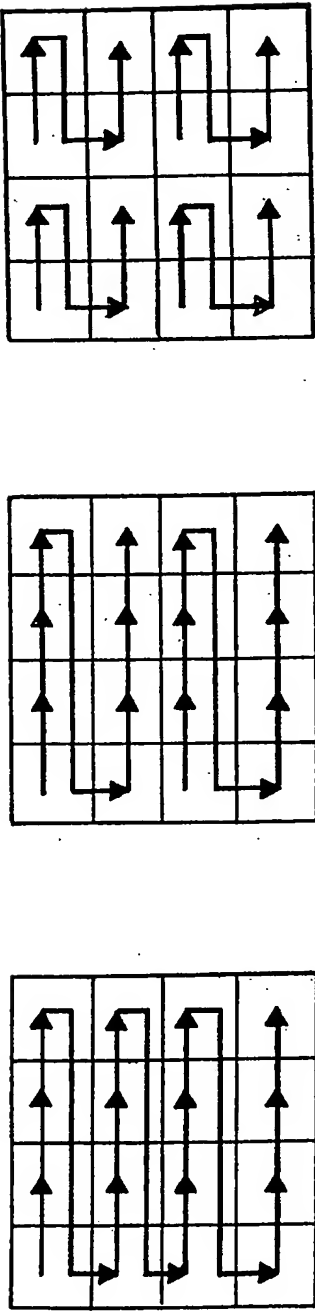


FIG. 21D



Single-Processor System

Two-Processor System

Four-Processor System

FIG. 22A

FIG. 22B

FIG. 22C

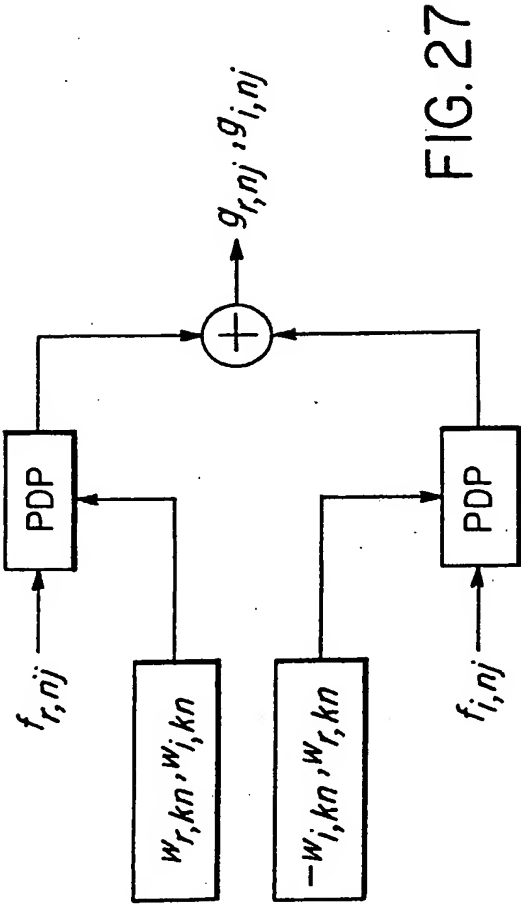
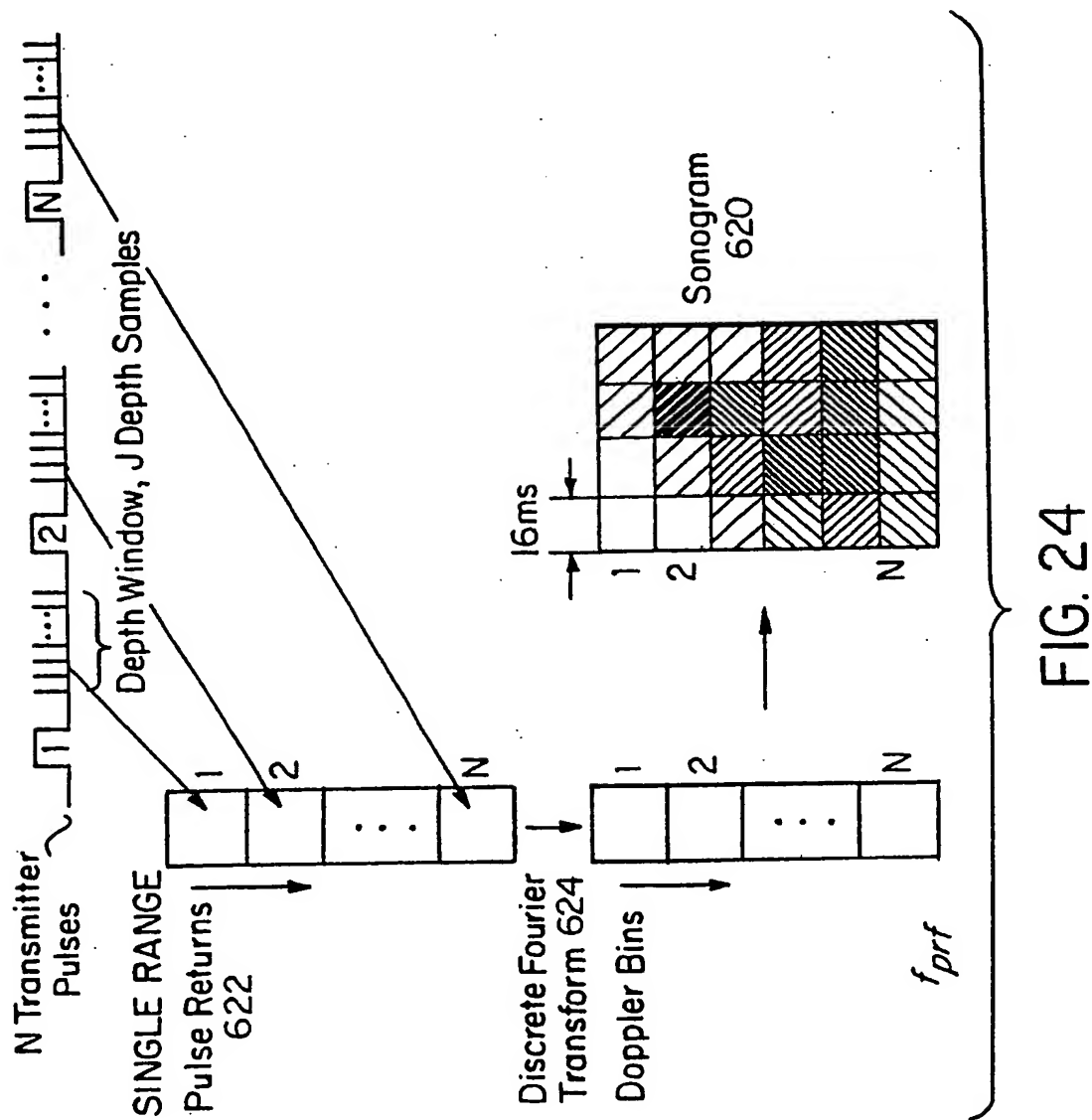


FIG. 27



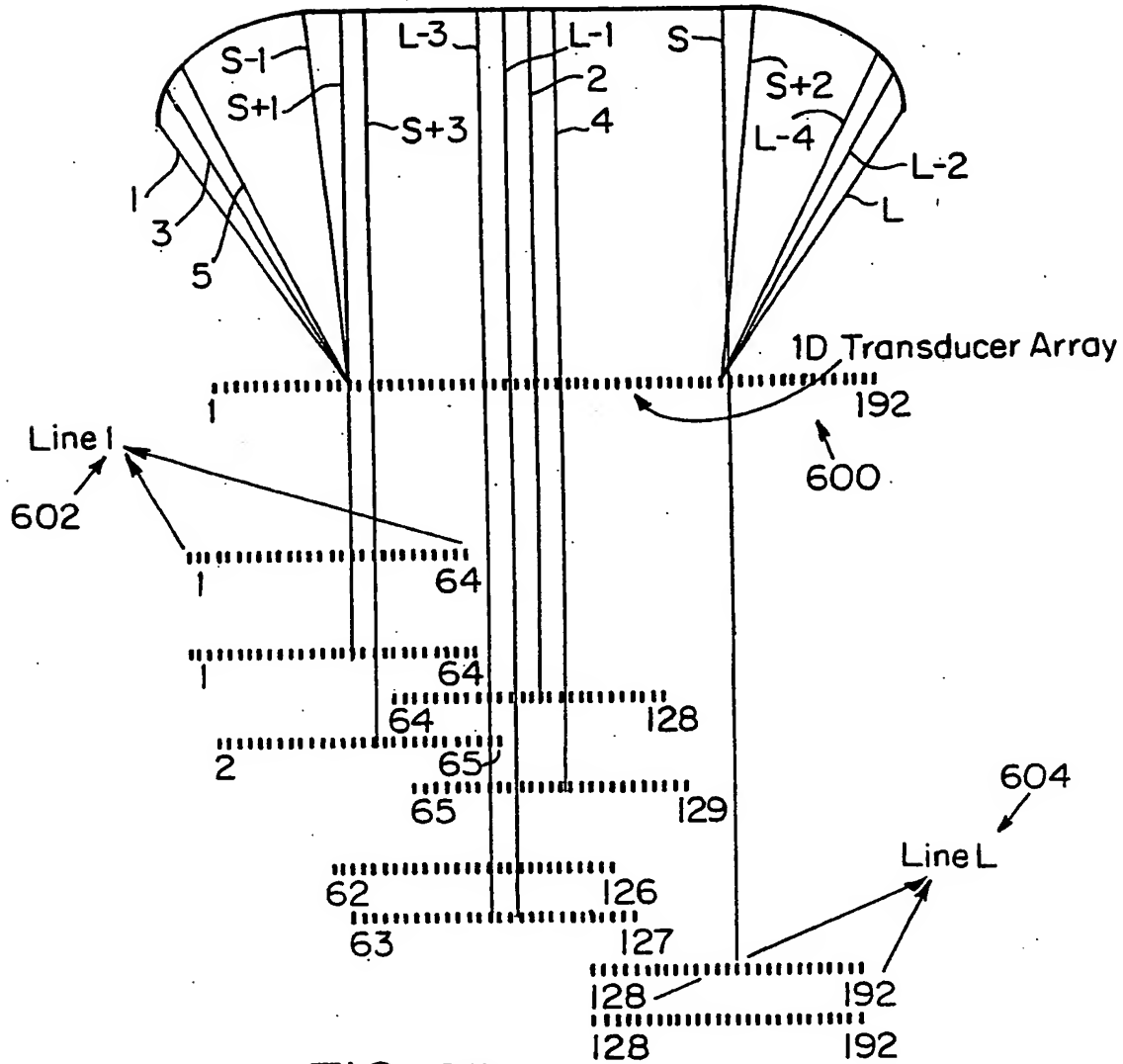


FIG. 23

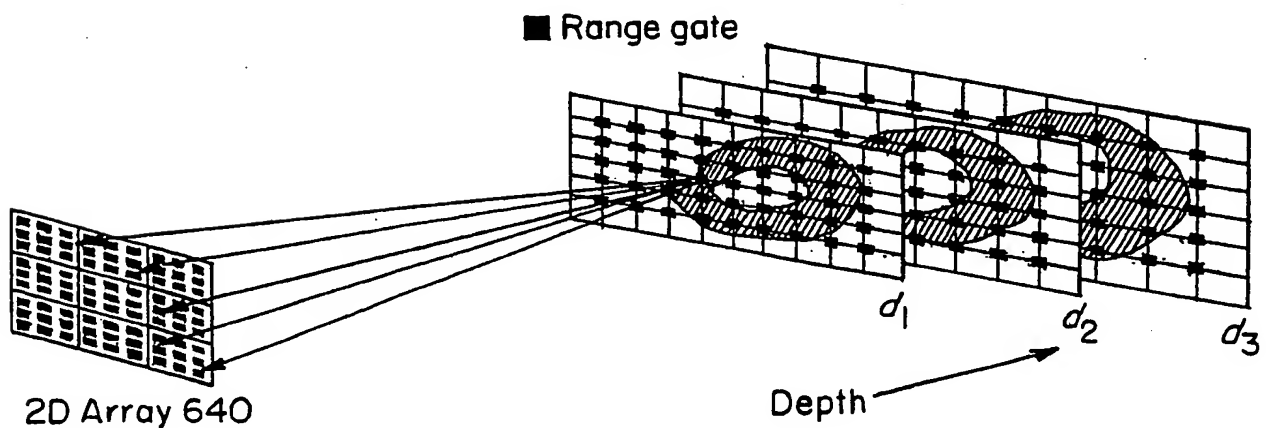


FIG. 25

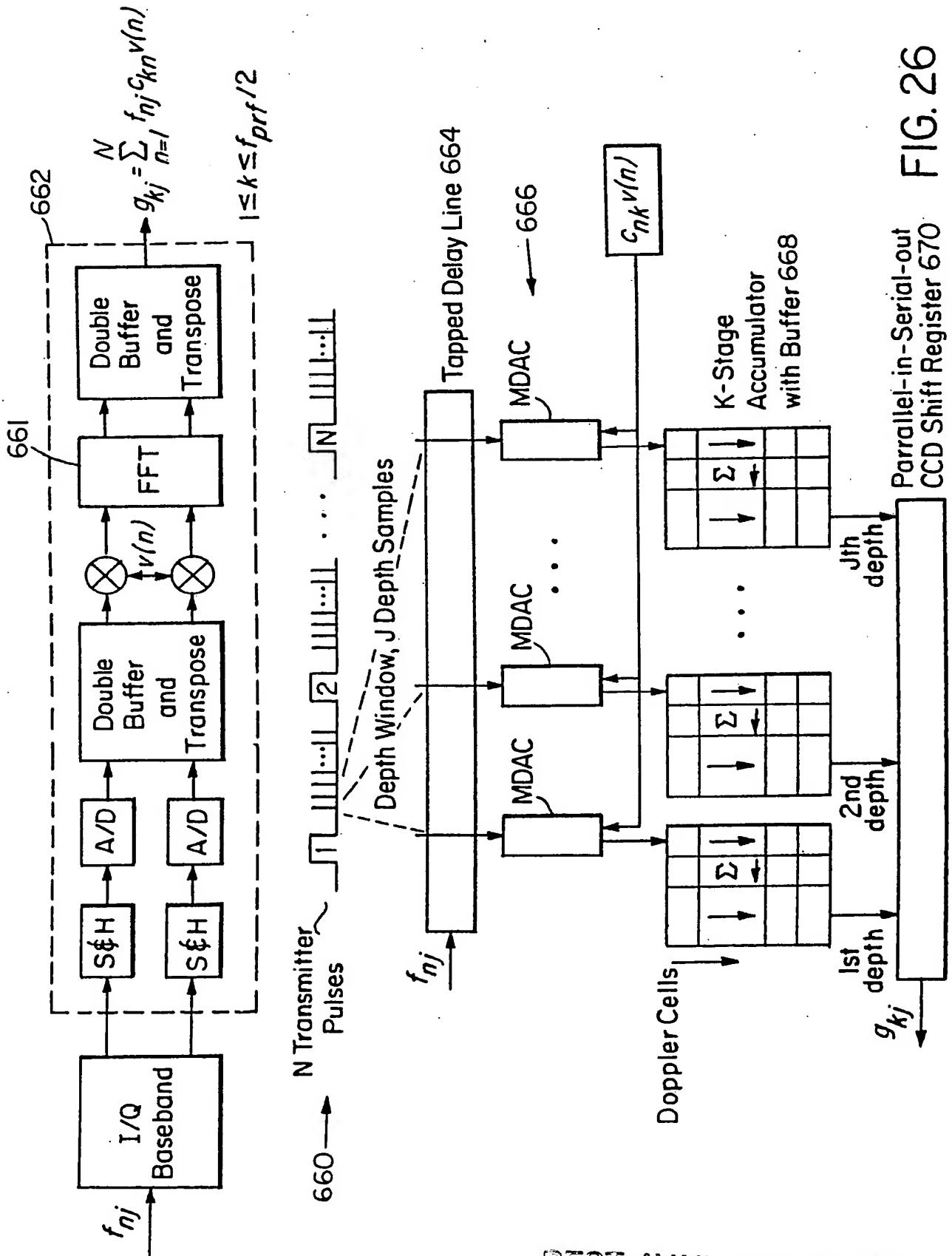


FIG. 26

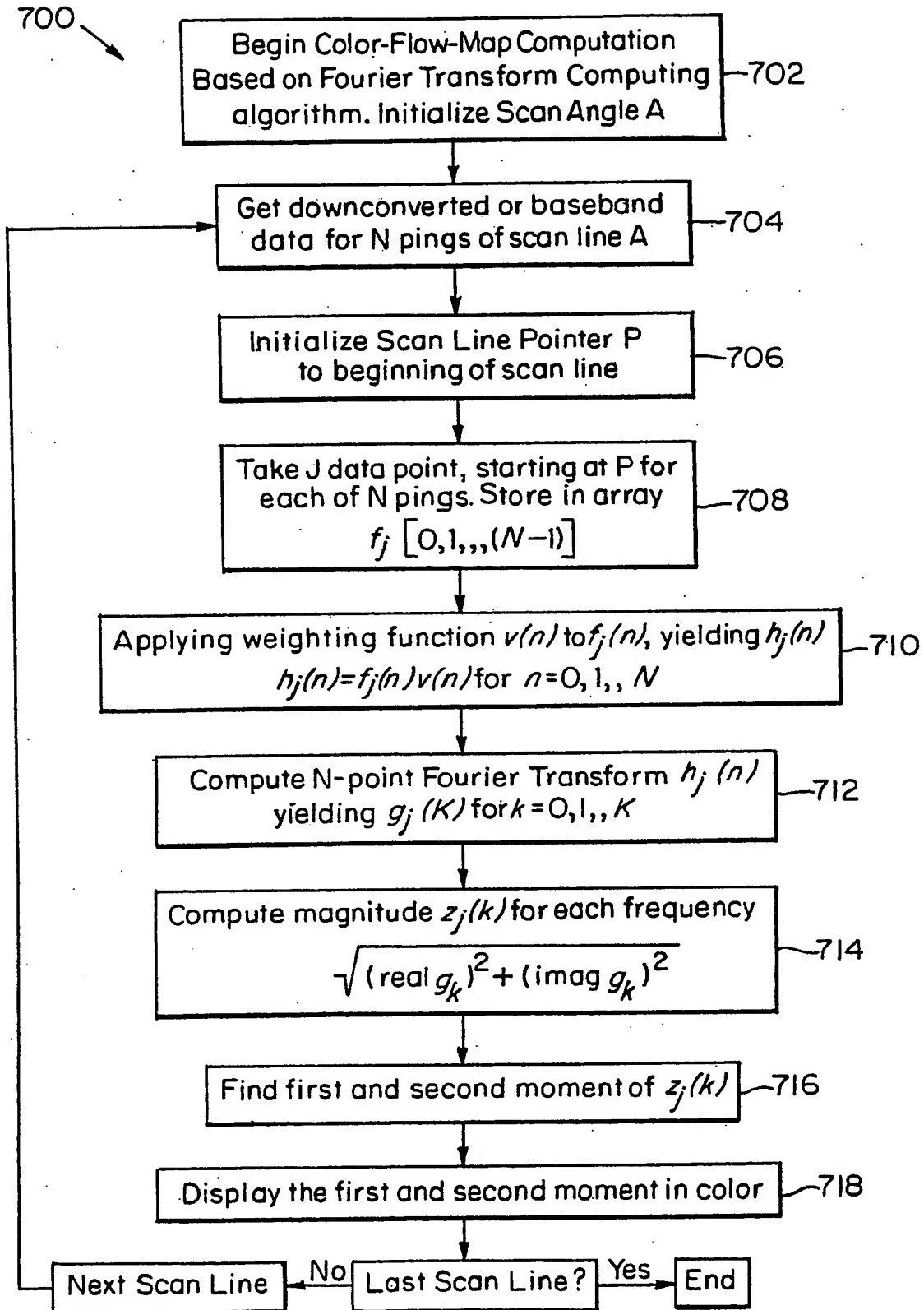


FIG. 28

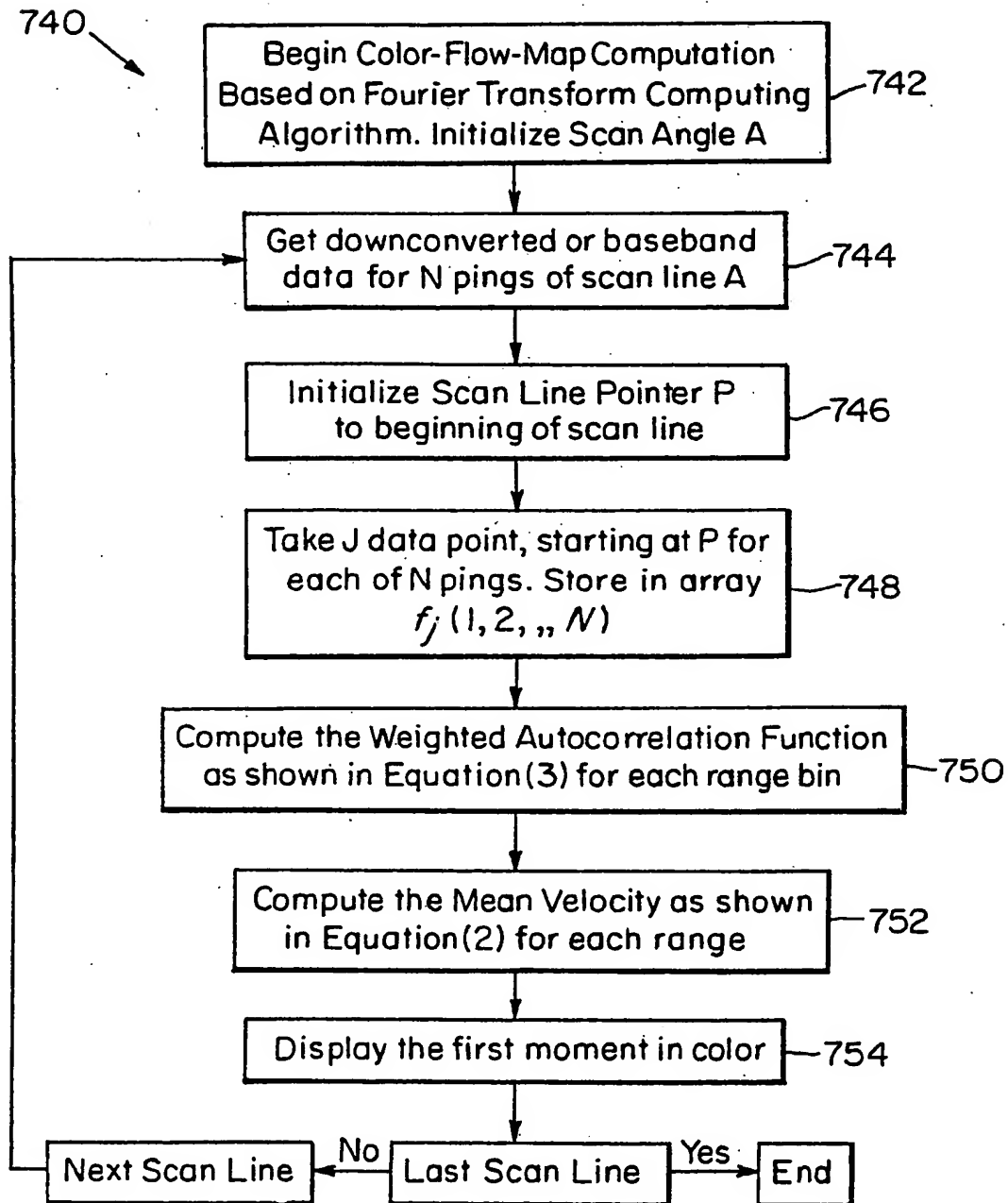


FIG. 29

